AG35 Series

Reference Design

Automotive Module Series

Version: 1.1

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Status: Released

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About the Document

Revision History

Version	Date	Author	Description
1.0	2017-12-27	Eden LIU	Initial
1.1	2021-05-31	Eden LIU	1. Deleted the SGMII interface design. 2. Sheet 1: Added the block diagram of AG35 series reference design. 3. Sheet 2: Updated the power supply block diagram. 4. Sheet 3: Modified the part number of L0101 common mode inductor to DLM11SN900HZ2L; deleted the test point circuit of USB; reserved pin 159; enabled pin 152 (MCLK) and pin 176 (SHDN_N) in U0101-B; updated the name of pins 132–141 in U0101-D for the optional audio function. 5. Sheets 3 and 9: Updated the ADC circuit for antenna detection. 6. Sheet 4: Removed pins USB_VBUS, USB_D+, USB_D- and USB_ID for U0201, updated the WAKEUP_IN circuit, and added the SHDN_N circuit. 7. Sheets 5 and 6: Updated the power supply designs for the AG35 series, AF20, PCM codec, PHY and the SD card interface; added the power supply design for antenna detection. 8. Sheet 7: Modified the part number of Q0501–Q0504 to 2SC4617. 9. Sheet 8: Optimized the design of reset delay circuit. 10. Sheet 9: Optimized the design of antenna interfaces by adding designs for antenna status detection. 11. Sheet 10: Updated the exterior trace length requirement of SDIO signal trace to 27 mm. 12. Sheet 11: Updated the AF20 antenna circuit, and deleted the pull-up circuit on pin 13 PCM_IN of AF20.

	13. Sheet 12: Updated STATUS and USB_BOOT circuits. 14. Sheet 13: Added the USB interface design.

Contents

1 Reference Design

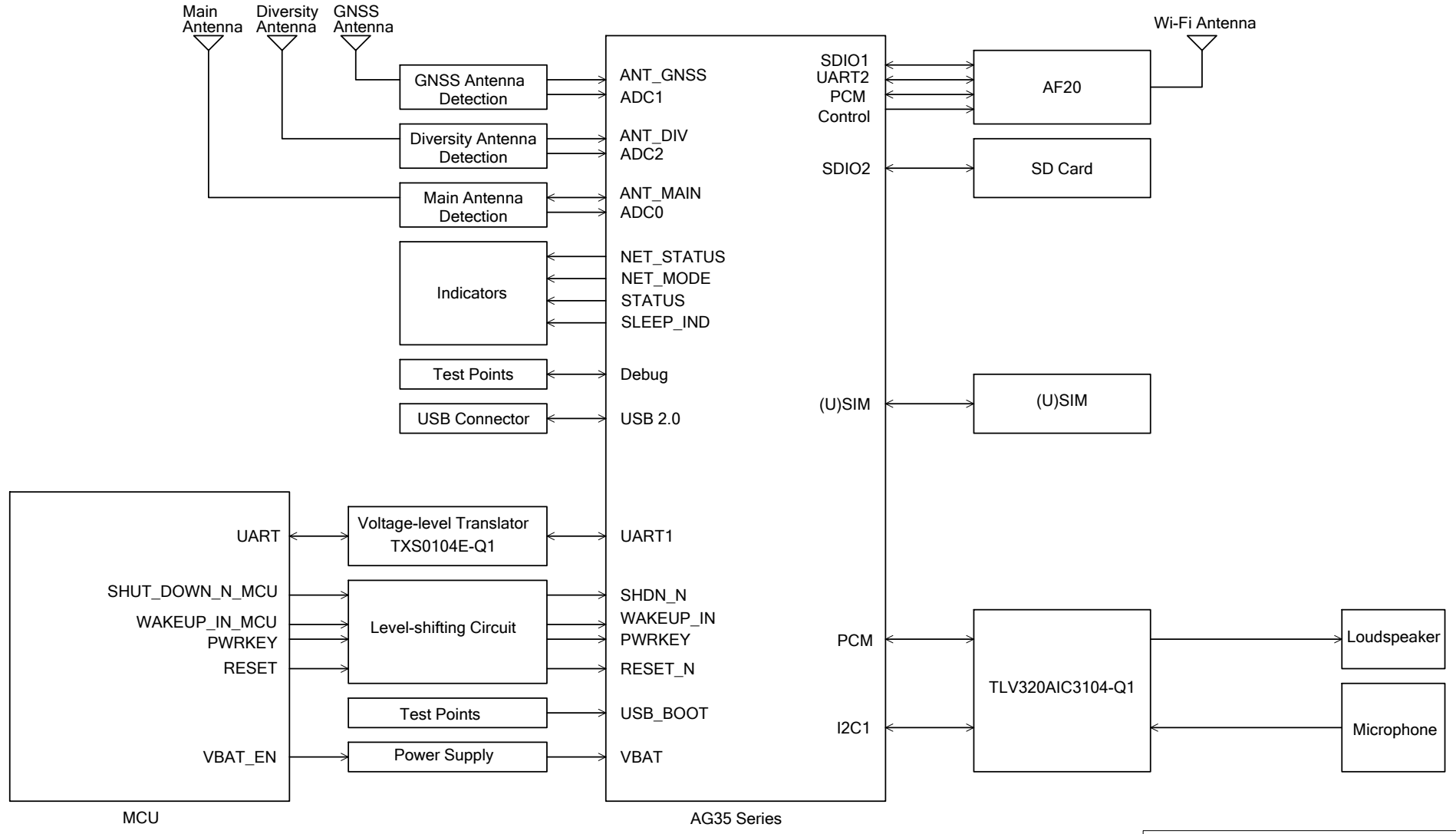
1.1. Introduction

This document provides the reference design for Quectel AG35 series module.

1.2. Schematics

The schematics illustrated in the following pages are provided for reference only.

Block Diagram



Note:
Power domain of the MCU is 3.3 V.

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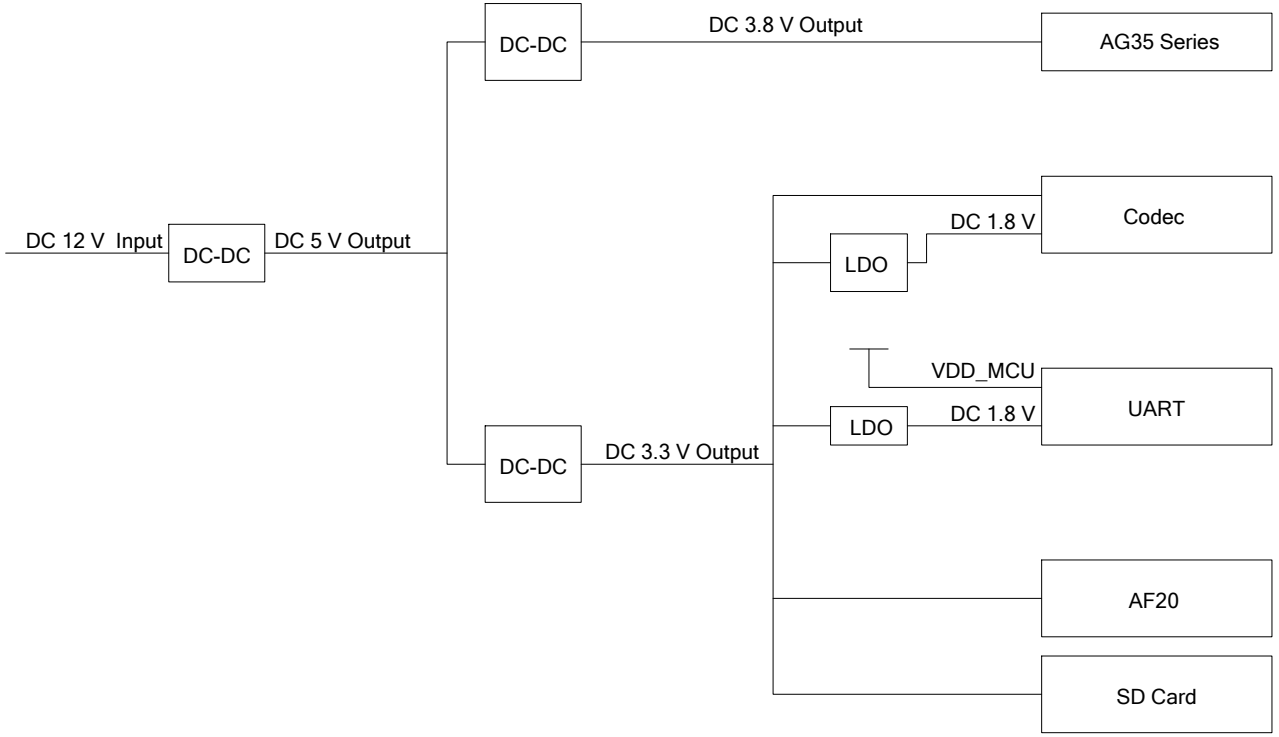
Power Supply Block Diagram



Note:
For DC-DC application, a DC-DC converter is used to convert a high input voltage into 5 V output, then covert the 5 V voltage into 3.8 V and 3.3 V outputs, and finally LDOs will generate 1.8 V typical voltages.

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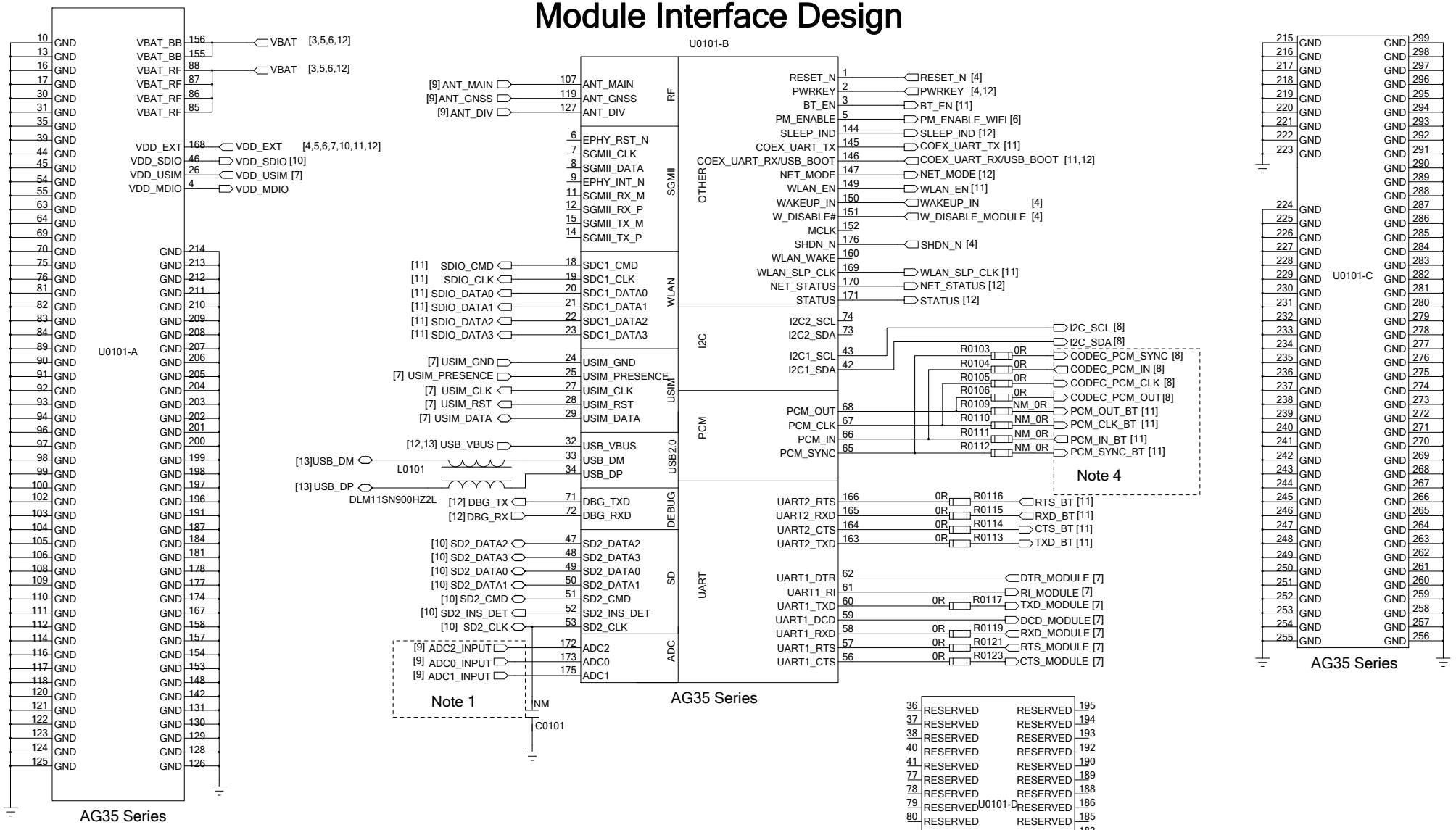
Module Interface Design



Notes:

1. ADC pins cannot be directly connected to the power supply and the input voltage for each ADC interface must not exceed its voltage range.
2. It is recommended to reserve the test points for firmware upgrade over USB interface and minimize the stub length of USB test signals.
3. Keep all RESERVED and unused pins unconnected, and ensure that all GND pins are connected to the ground network.
4. PCM_xxx_BT network is used for communication with AF20 module. CODEC_PCM_xxx network is used for communication with external codec. AF20 and codec cannot be connected to the same PCM interface simultaneously.
5. Pins 145-147 and 149 must be at low level before the module starts up successfully.

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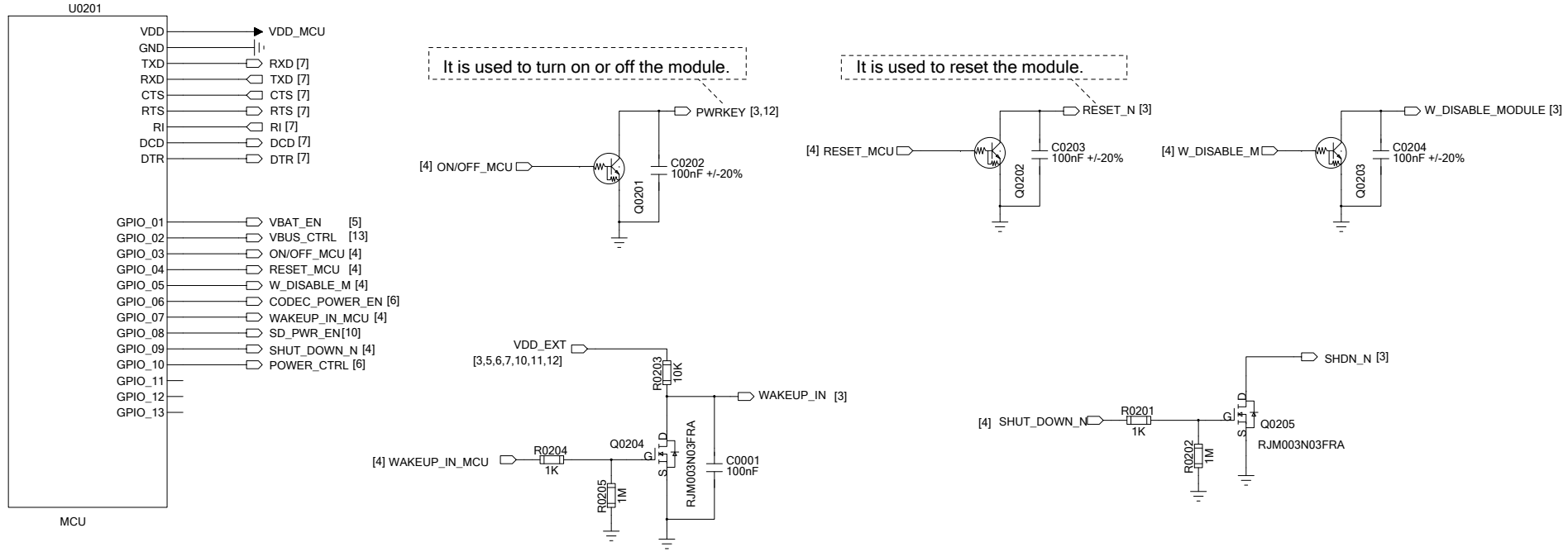
MCU Interface Design



Notes:

1. U0201 represents the MCU.
2. AG35 series module can only work as a USB device and it supports Full Speed and High Speed modes. To communicate through USB interface, MCU needs to support USB host or OTG function. The VBUS pins of MCU and AG35 series module should be powered by a 5 V power system for USB detection, and VBUS_CTRL is used to turn on/off VBUS power supply. When VBUS_CTRL is at high level, USB_VBUS will be powered on.

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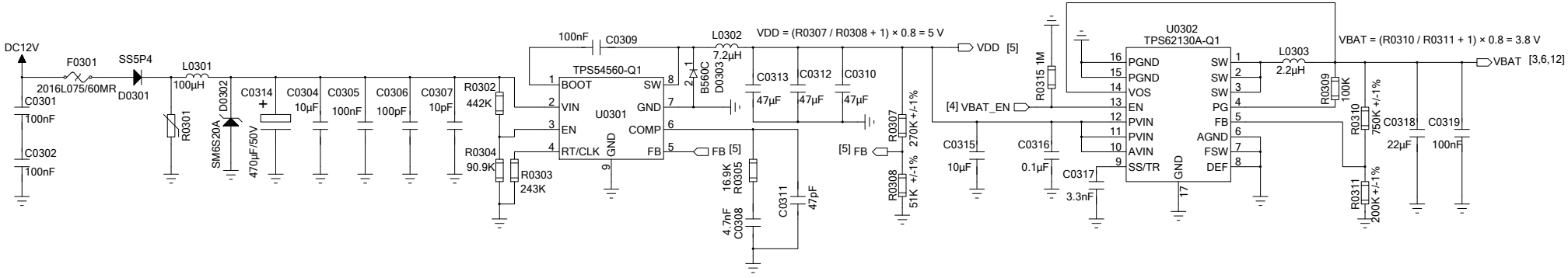
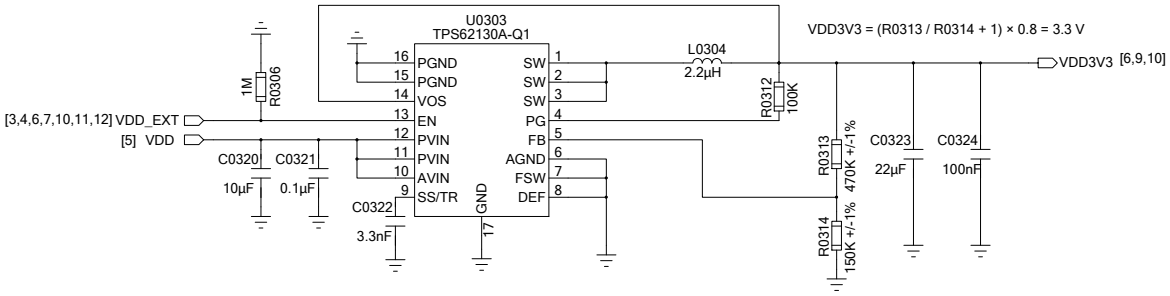
Power Supply Designs (Part 1)

Module Power Supply



Codec/PHY/AF20/SD Power Supply



Notes:

1. The power supply must be able to provide a sufficient current of 3 A at least.
2. VBAT_EN is used to control power supply of the module. It is at high level by default when the module is in a state of power supply. When VBAT_EN is at low level, VBAT power supply will be switched off.

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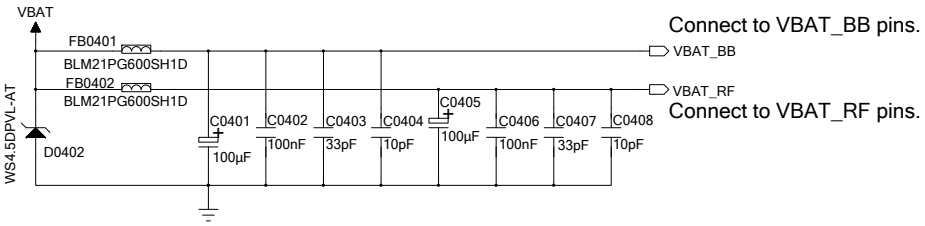
Power Supply Designs (Part 2)

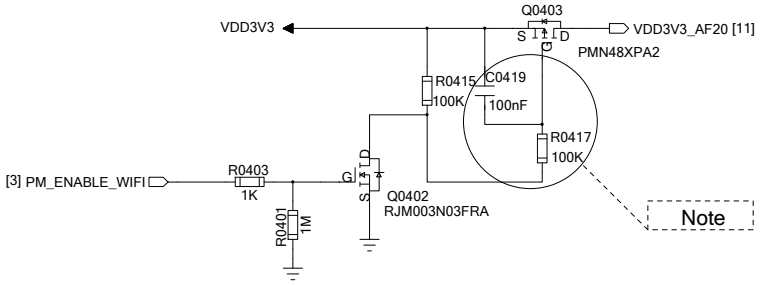
VBAT Design



Notes:

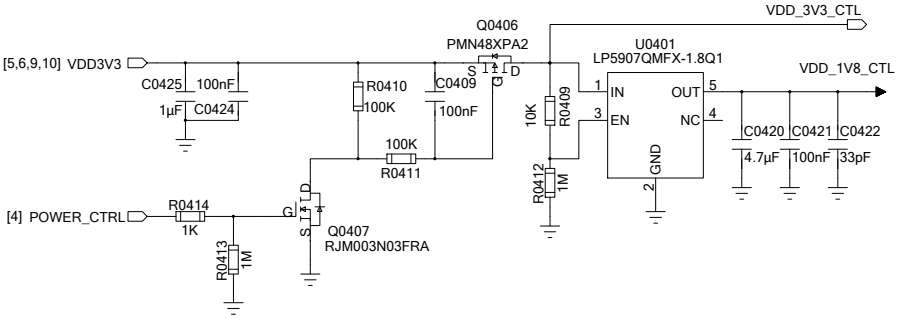
1. The power supply must be able to provide a sufficient current of 2 A at least.
2. VBAT_BB and VBAT_RF pins should be routed in star structure.
3. The recommended operating voltage of VBAT is 3.3-4.3 V.
4. The capacitors C0401-C0408 should be placed close to the module's VBAT pins.

Power Supply for AF20

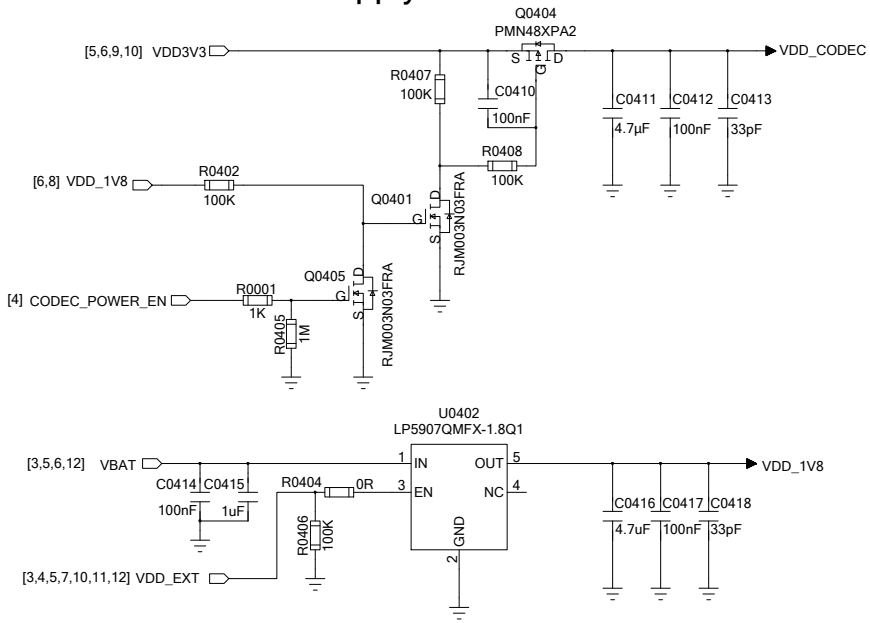


Note:
The RC circuit, assembled with R0417 and C0419, is used to delay the start-up of MOSFET switch circuit.

Power Supply for Antenna Detection



Power Supply for PCM Codec



Note:
CODEC_POWER_EN must be at low level to ensure normal operation of PCM codec.
If VDD_CODEC power supply needs to be switched off, keep CODEC_POWER_EN at high level.

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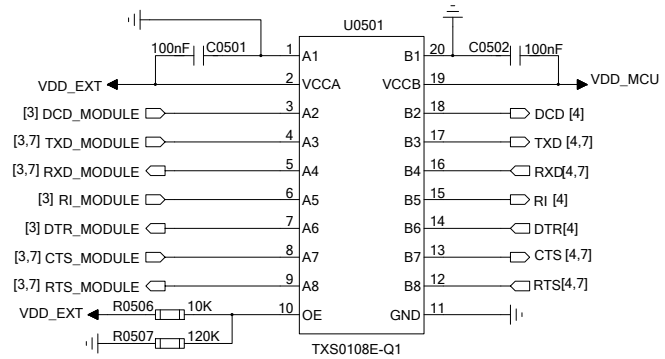
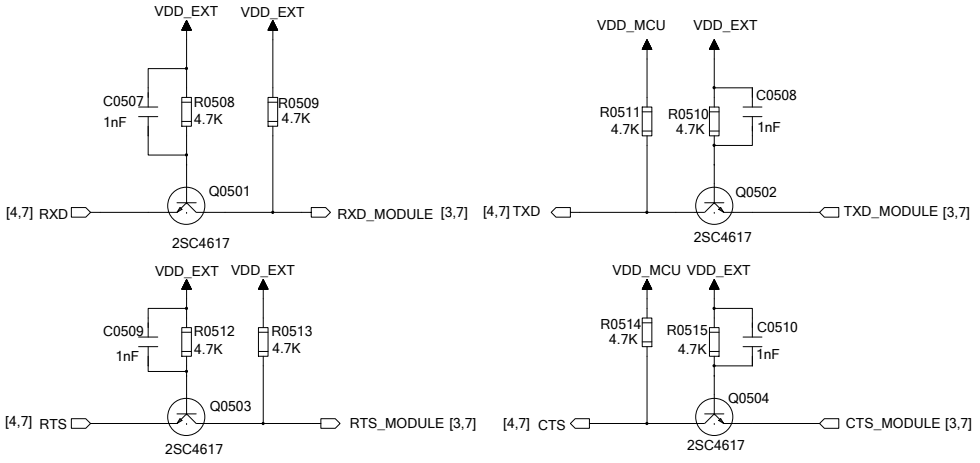
(U)SIM and UART Interfaces Design

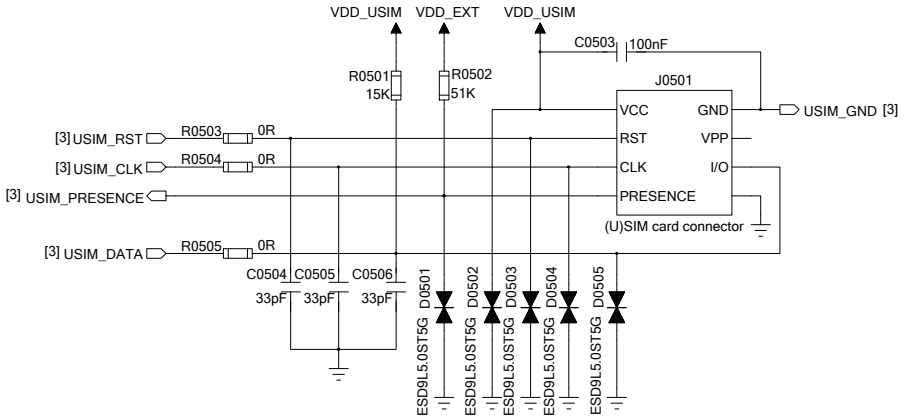
UART Level-shifting Circuit - IC Solution (Recommended)



UART Level-shifting Circuit - Transistor Solution



(U)SIM Interface



Notes:

1. The decoupling capacitor of VDD_USIM should be less than 1 μF and must be near to (U)SIM card connector.
2. AG35 series module provides an input pin (USIM_PRESENCE) to detect the (U)SIM card.
   It supports both low level and high level detection.
   For more details, see *Quectel_AG35_Hardware_Design*.
3. R0503-R0505 are applied to suppress the EMI spurious transmission and enhance the ESD protection.
4. It is recommended to take electrostatic discharge (ESD) protection measures near the (U)SIM card connector. The TVS diode with junction capacitance less than 10 pF must be placed as close to the (U)SIM card connector as possible.
5. R0501 can improve anti-jamming capability of the (U)SIM interface circuit and it should be placed close to the (U)SIM card connector.

Notes:

1. It is recommended to use the IC solution for voltage-level translation.
   The transistor solution is not suitable for applications with high baud rates exceeding 460 kbps.
2. The supply voltage range of VCCA should not exceed that of VCCB. For more information about TXS0108E-Q1, refer to the datasheet from Texas Instruments.
3. If high baud rate is needed, it is highly recommended to install four 1 nF capacitors (C0507/C0508/C0509/C0510) on transistor circiuts.
4. The DTR transistor circuit is similar to that of RTS. The RI and DCD transistor circuits are similar to that of CTS.

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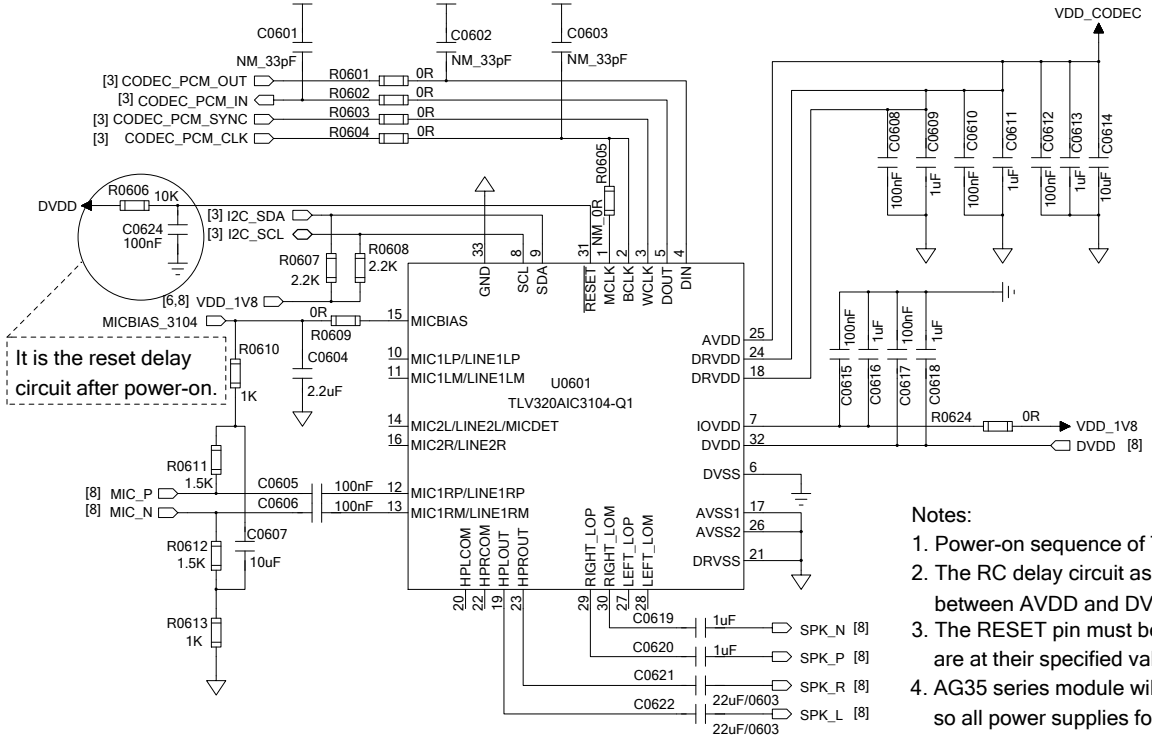
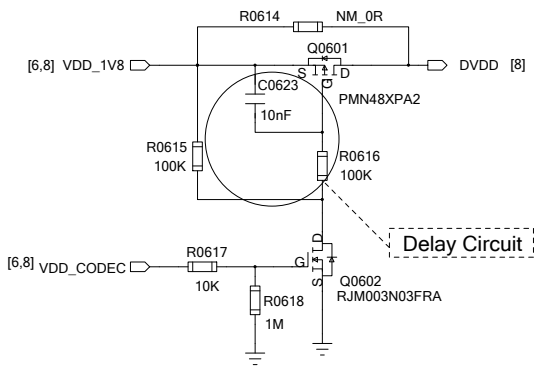
Audio Design

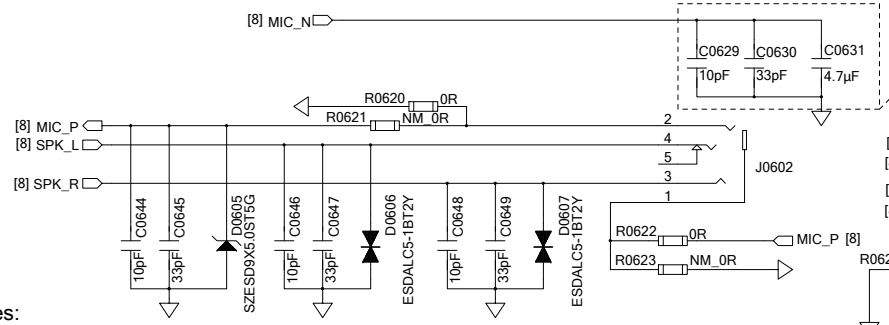




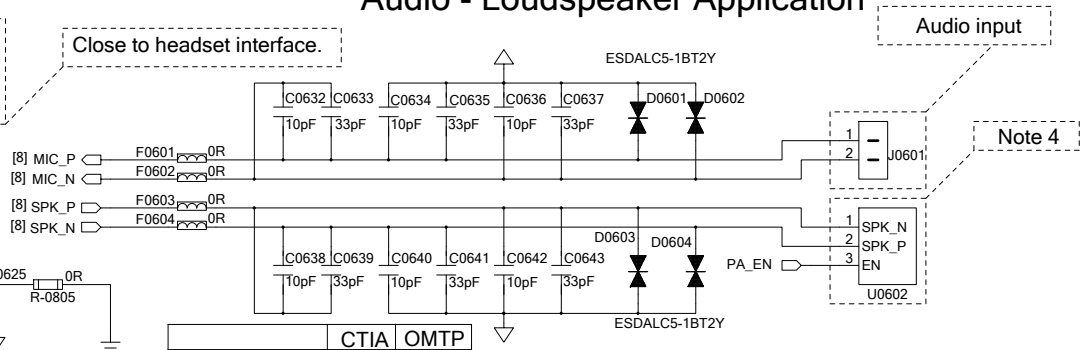
Notes:

1. Power-on sequence of TLV320AIC3104-Q1: IOVDD → AVDD/DRVDD → DVDD → Software Initialization.
2. The RC delay circuit assembled with C0623 and R0616 is used to ensure that the power-on time difference between AVDD and DVDD is within 5 ms. For more details, refer to TLV320AIC3104-Q1 datasheet.
3. The RESET pin must be at low level for at least 10 ns after all power supplies for TLV320AIC3104-Q1 are at their specified values.
4. AG35 series module will automatically initialize the codec via I2C1 interface after the module is turned on successfully, so all power supplies for the codec need to be turned on before that.

Audio - Headset Application



Audio - Loudspeaker Application



	CTIA	OMTP
R0621/R0623	NM	M
R0620/R0622	M	NM

Notes:

1. The analog output only drives headset. For larger power loads such as loudspeakers, an audio power amplifier should be added in the circuit design.
2. The analog GND should be connected to the main GND via the 0 Ω resistor (R0625).
3. The maximum capacitive load of SPK_N/P for speaker is 330 pF and the maximum capacitive load of MIC_N/P for microphone is 250 pF.
4. U0602 is a simplified loudspeaker output circuit of an external power amplifier. To suppress POP, it is recommended to control the external power amplifier through PA_EN, enabling it to be turned on after the module's audio function is established.

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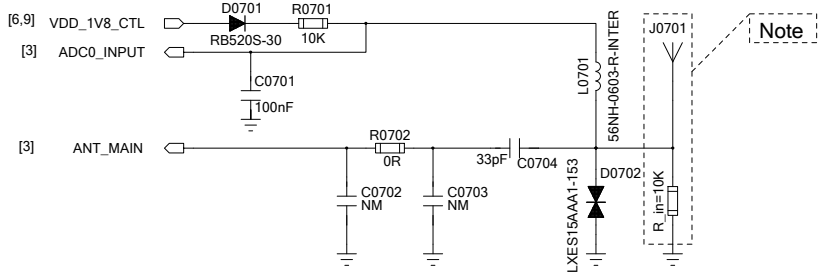
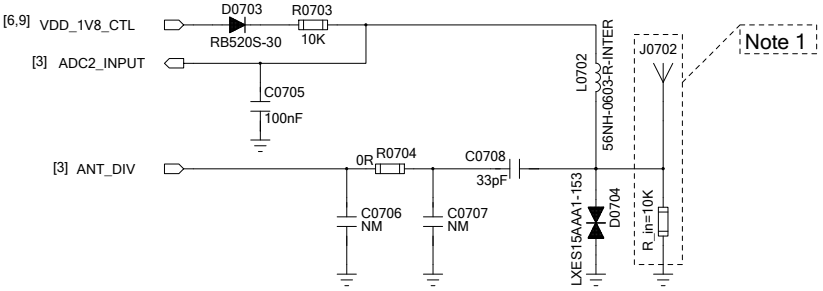
Antenna Interface and Antenna Detection Circuit Design

Main Antenna Interface and Detection Circuit (Normal)



Note:
To detect antenna status successfully, the main antenna is recommended to integrate an 8-13 kΩ resistor (R_in) to GND. And the typical value for the resistor is 10 kΩ.

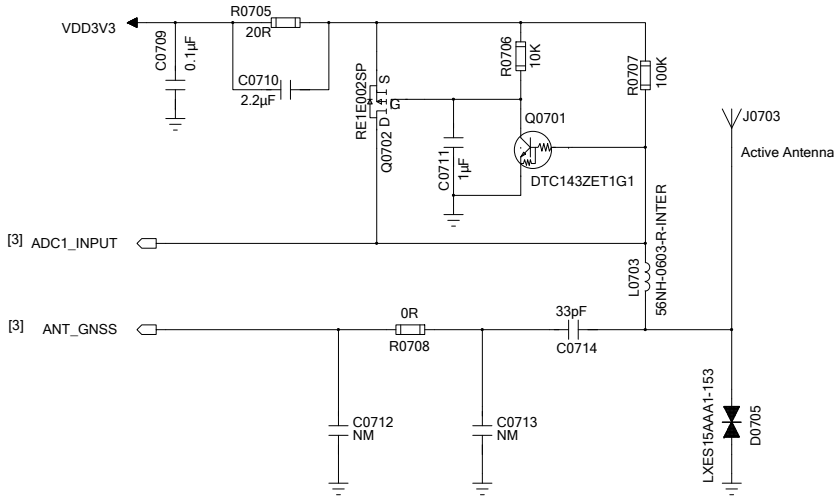
Rx-diversity Antenna Interface and Detection Circuit (Normal)



Notes:
1. To detect antenna status successfully, the Rx-diversity antenna is recommended to integrate an 8-13 kΩ resistor (R_in) to GND. And the typical value for the resistor is 10 kΩ.
2. The Rx-diversity reception function is ON by default. If Rx-diversity antenna is not used, use AT command to turn off Rx-diversity reception.

Main/Rx-diversity Antenna Status Indication					
Antenna Status	Open	R_in = 8 kΩ	R_in = 10 kΩ	R_in = 13 kΩ	Short to GND
ADC Value	1.7 V	0.7 V	0.8 V	0.9 V	0 V
Status Indication	Open	Normal	Normal	Normal	Short to GND

GNSS Antenna Interface and Detection Circuit (Normal)



GNSS Antenna Status Indication			
Antenna Status	Open	Normal	Short to GND
ADC Value	VDD3V3	VDD3V3 - R0705 × I_GNSS	0 V

Notes:
1. It is recommended to select a low power active antenna.
2. An external LDO can be selected to supply power according to the active antenna requirement.
3. VDD3V3 is the power supply for active antenna, and I_GNSS is the opearting current of active antenna.
4. The active antenna power supply shall not exceed VBAT voltage of the module. And ADC0 or ADC1 shall be selected for ADC value detection.

Notes:
1. It is recommended to use π type main/Rx-diversity antenna circuit to facilitate future debugging.
2. The impedance of the RF signal traces must be controlled as 50 Ω when routing.
3. ADC value can be read by AT+QADC=<port>. For more details, see *Quectel_AG35_AT_Commands_Manual*.
4. Three kinds of antenna status are designed to be detected: Normal, Short to GND and Open.
5. The antenna connection status is judged by the voltage detected on the ADC pins.

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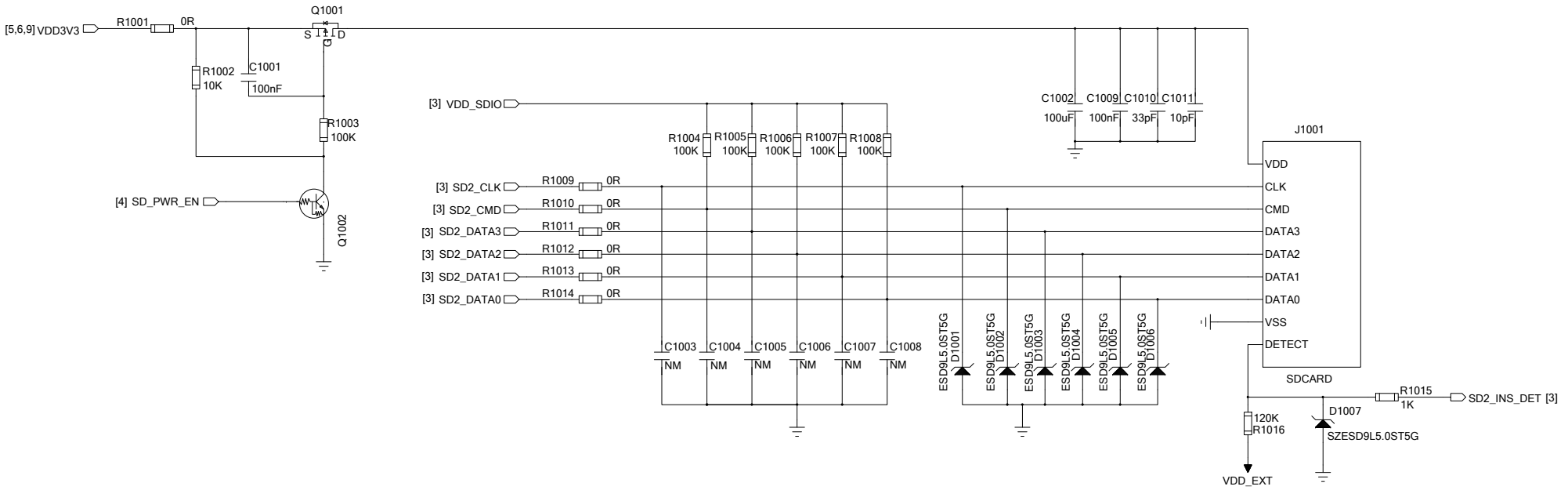
SD Card Interface Design



Notes:

1. VDD_SDIO can only be used for SDIO pull-up resistors and its maximum output current is 50 mA.
2. The supply voltage range of VDD for SD card interface is 2.7-3.6 V and sufficient current up to 0.8 A should be provided.
3. To avoid jitter of bus, resistors R1004-R1008 are needed to pull up the SDIO to VDD_SDIO. The value of these resistors is among 10-100 kΩ and the recommended value is 100 kΩ.
4. To improve signal quality, it is recommended to add 0 Ω resistors R1009-R1014 in series between the module and the SD card connector.
   The bypass capacitors C1003-C1008 are reserved and not mounted by default. All resistors and bypass capacitors should be placed close to the module.
5. It is recommended to add ESD protection devices near the pins of SD card connector. The parasitic capacitance of ESD protection devices should be smaller than 2 pF.
6. Keep SDIO signals far away from other sensitive circuits/signals such as RF circuits and analog signals, as well as noisy signals such as clock signals and DC-DC signals.
7. Route SD card signal traces with 50 Ω impedance, and it is important to route the SDIO signal traces with total grounding.
8. Make sure the adjacent trace spacing is two times of the trace width and the bus capacitance is less than 40 pF.
9. It is recommended to keep the trace length difference between CLK and DATA/CMD less than 1 mm. The total trace length inside the module is 23 mm, so the exterior total trace length should be less than 27 mm.
10. The pin DETECT of SD card connector must be connected to the module when SD card function is used.

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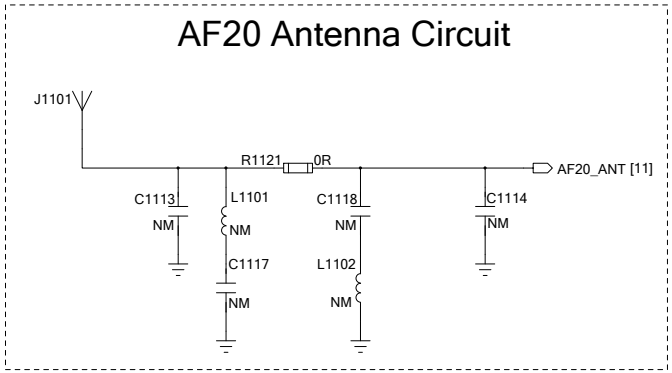
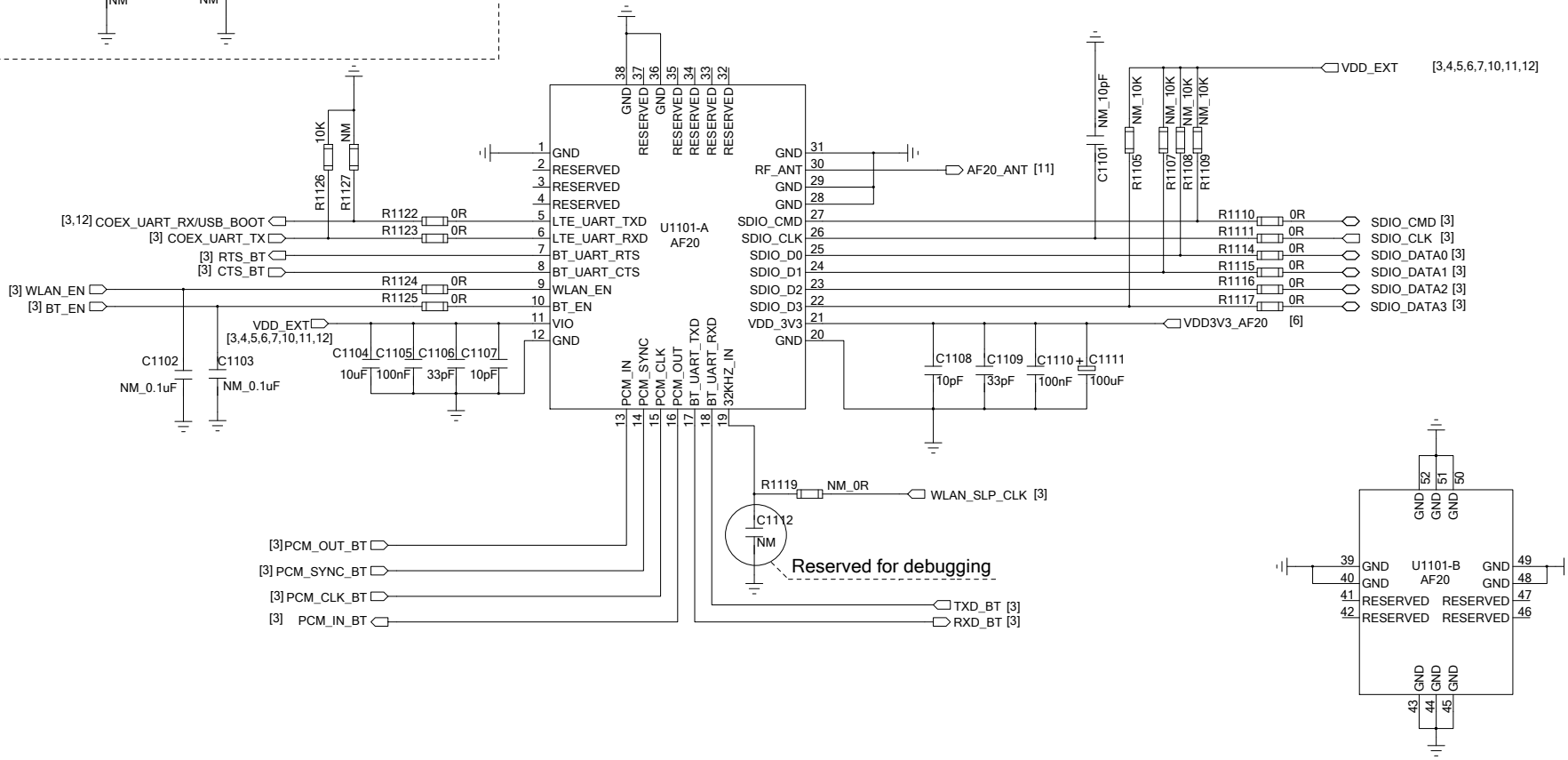
AF20 Design





Notes:

1. Keep all RESERVED and unused pins unconnected.
2. The impedance of the SDIO data signal traces must be controlled as 50 Ω when routing.
3. SDIO data traces should be surrounded by ground; SDIO_CMD and SDIO_CLK signal traces should be surrounded by ground seperately.
4. It is recommended to use π type circuit for AF20 antenna design for future debugging purpose.
5. The impedance of RF signal trace must be controlled as 50 Ω when routing.

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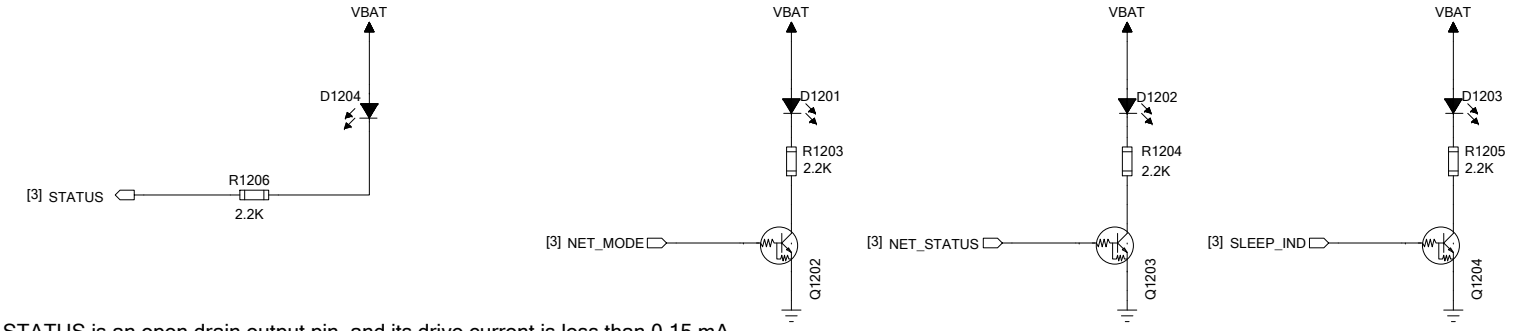
Indicators and Test Points Designs

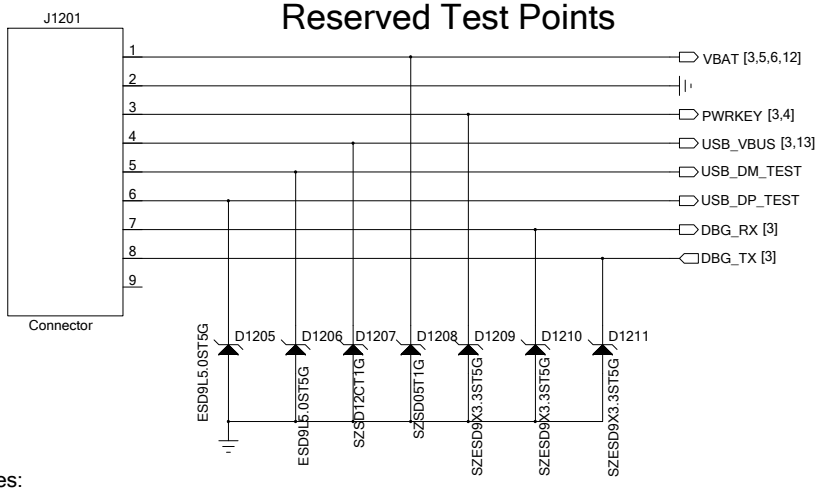
Indicators



Notes:

1. The STATUS is an open drain output pin, and its drive current is less than 0.15 mA.
2. For more details about NET_MODE and NET_STATUS, see *Quectel_AG35_Hardware_Design*.
3. If minimized power consumption is required when the device is in sleep mode, it is recommended to replace the power supply of indicators with a controllable one, and use it to turn off the power supply when the module enters sleep mode.

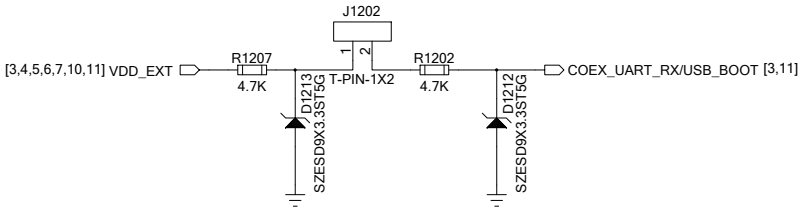
Reserved Test Points



Notes:

1. Reserve the test points of USB and debug UART interfaces for software debugging.
2. USB interface also can be used to upgrade firmware.
3. Keep USB test points as close as possible to USB pins.
   Pay attention to the junction capacitance of ESD protection devices on USB data traces, which might influence the signal. Typically, the capacitance value should be less than 2 pF.
4. Debug UART interfaces support 1.8 V power domain.
   A voltage-level translator should be used if the power domain of your application is 3.3 V.

USB_BOOT for Download



Note:

COEX_UART_RX/USB_BOOT is kept open by default and the module will be forced into emergency download mode when COEX_UART_RX/USB_BOOT is at high level during module power-up.

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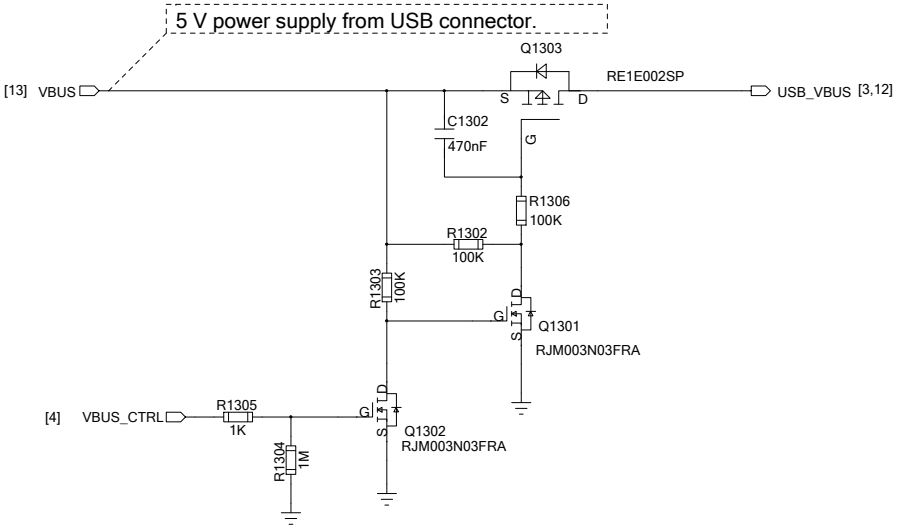
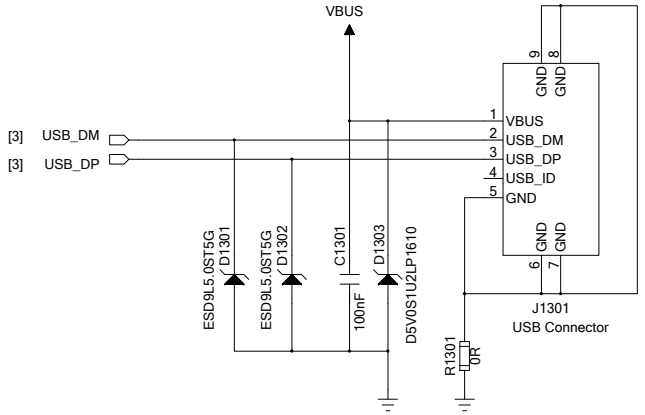
USB Interface Design





Notes:

1. The USB_VBUS pin of AG35 series should be powered by a 5 V power system for USB detection.
2. USB interface can be used for debugging and firmware upgrading.
3. Pay attention to the junction capacitance of ESD protection devices on USB data traces, which might influence the signal. Typically, the value of capacitance should be less than 2 pF.
4. USB_VBUS should be controlled by USB host.
   VBUS_CTRL controlled by MCU is used to turn on/off USB_VBUS power supply.
   VBUS_CTRL is at low level by default. When it is at high level, USB_VBUS will be switched off.

Quectel Wireless Solutions		
DRAWN BY Eden LIU	PROJECT AG35 Series	TITLE Reference Design
CHECKED BY Yeoman CHEN	SIZE A2	VER 1.1
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