EC20 R2.1
Reference Design

LTE Module Series

Rev. EC20_R2.1_Reference_Design_Rev.A

Date: 2018-01-16

Status: Released

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About the Document

History

Revision	Date	Author	Description
A	2018-01-16	Lorry XU/ Woody WU	Initial

Contents

1 Reference Design

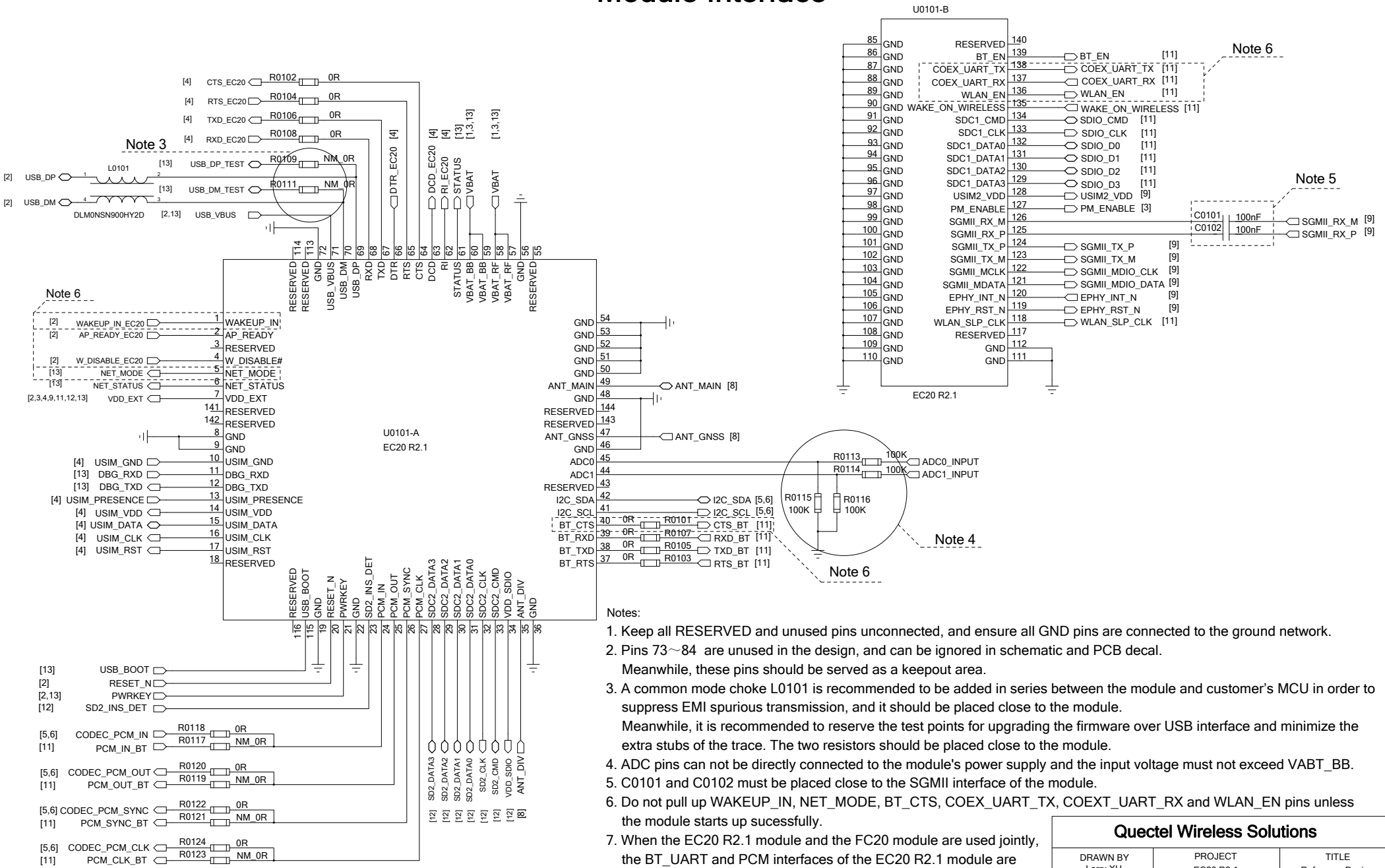
1.1. Introduction

This document provides the reference design for Quectel EC20 R2.1 module.

1.2. Schematics

The schematics illustrated in the following pages are provided for your reference only.

Module Interface



Notes:

1. Keep all RESERVED and unused pins unconnected, and ensure all GND pins are connected to the ground network.
2. Pins 73～84 are unused in the design, and can be ignored in schematic and PCB decal.
   Meanwhile, these pins should be served as a keepout area.
3. A common mode choke L0101 is recommended to be added in series between the module and customer's MCU in order to suppress EMI spurious transmission, and it should be placed close to the module.
   Meanwhile, it is recommended to reserve the test points for upgrading the firmware over USB interface and minimize the extra stubs of the trace. The two resistors should be placed close to the module.
4. ADC pins can not be directly connected to the module's power supply and the input voltage must not exceed VABT_BB.
5. C0101 and C0102 must be placed close to the SGMII interface of the module.
6. Do not pull up WAKEUP_IN, NET_MODE, BT_CTS, COEX_UART_TX, COEXT_UART_RX and WLAN_EN pins unless the module starts up sucessfully.
7. When the EC20 R2.1 module and the FC20 module are used jointly, the BT_UART and PCM interfaces of the EC20 R2.1 module are connected to the FC20 module BT_UART and PCM interfaces respectively.

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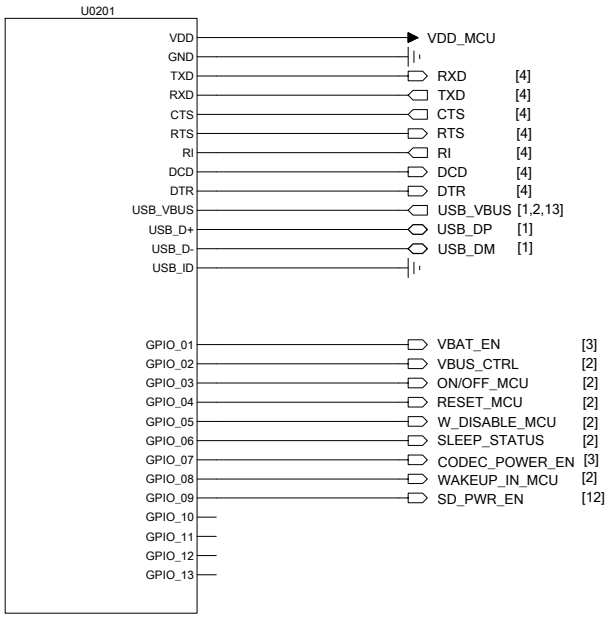
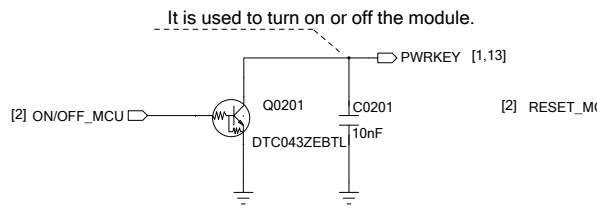
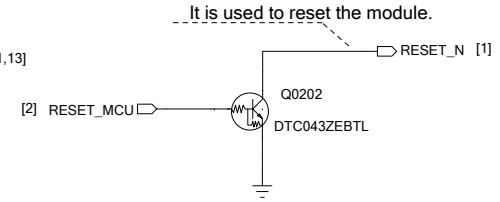
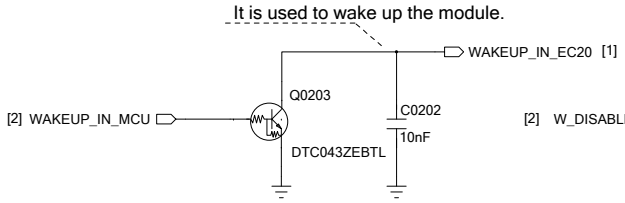
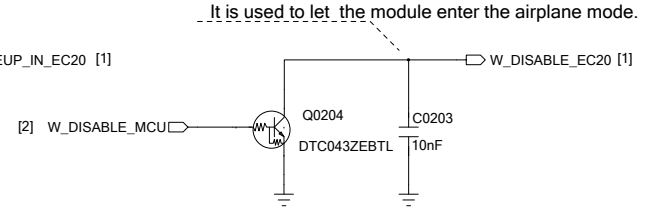
MCU Interface

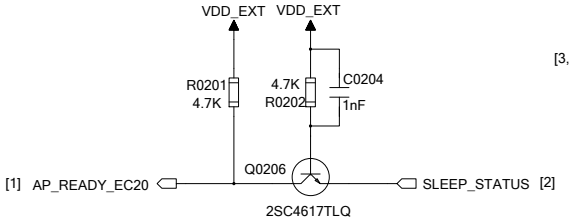


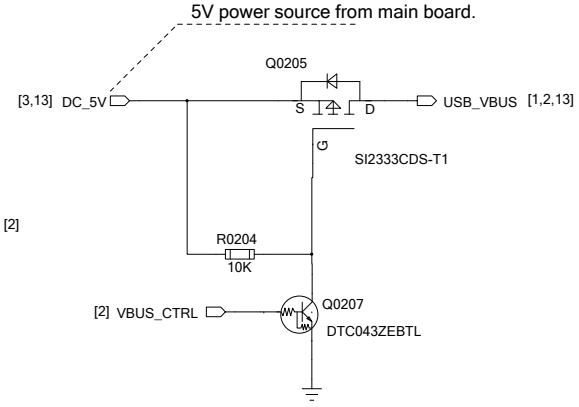












Notes:

1. U0201 represents customer's MCU. The power domain of GPIO interfaces on EC20 R2.1 modules is 1.8V, if the domain on U0201's GPIO interfaces is the same, then the level translation circuit can be omitted.
2. EC20 R2.1 can only work as a USB device and supports Full Speed and High Speed modes. To communicate with USB interface, MCU needs to support USB host or OTG function. The USB_VBUS pins of MCU and EC20 R2.1 should be powered by a 5V power system for USB detection, and VBUS_CTRL is used to turn on/off USB_VBUS power supply.
3. AP_READY is used to detect the MCU's sleep state. For more details, please refer to *Quectel_EC20_R2.1_Hardware_Design.*
4. WAKEUP_IN_EC20 should should be kept at low level before the module starts up successfully.

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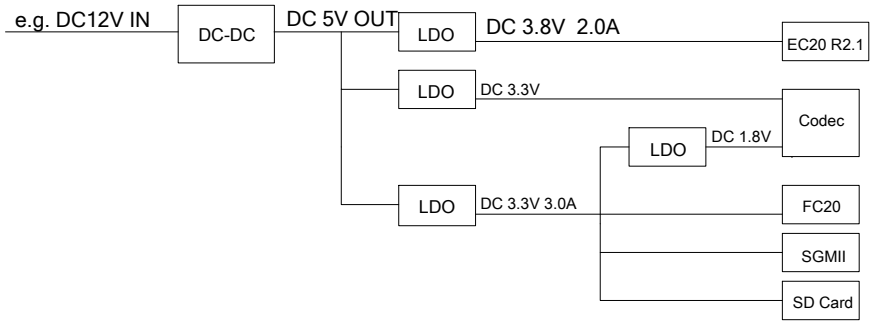
Power Supply Design

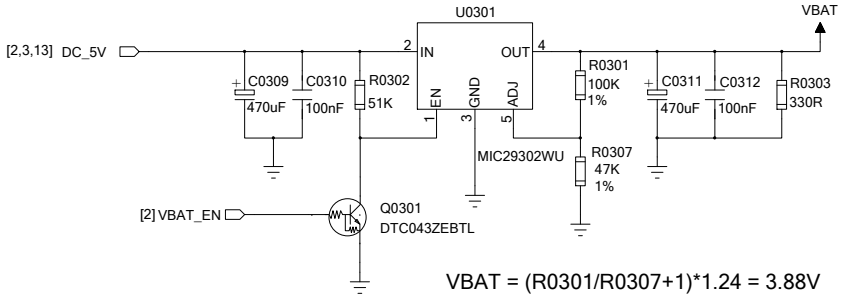
DC-DC Application

It is used when the input voltage is above 7V. Use a DC-DC converter to convert a high input voltage into a 5V output, and then the LDOs will generate 3.8V, 3.3V and 1.8V typical voltages.



LDO Application

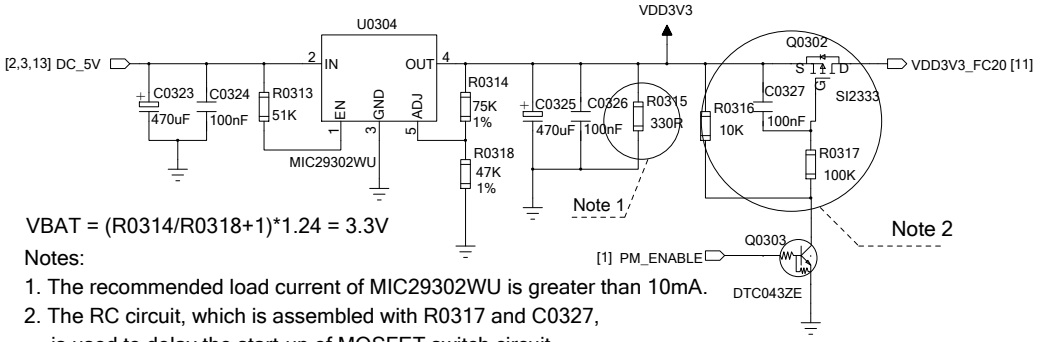
It is used when the input voltage is below 7V.



VBAT = (R0301/R0307+1)*1.24 = 3.88V

The recommended load current is greater than 10mA.

Power Supply for FC20, SGMII and SD Card

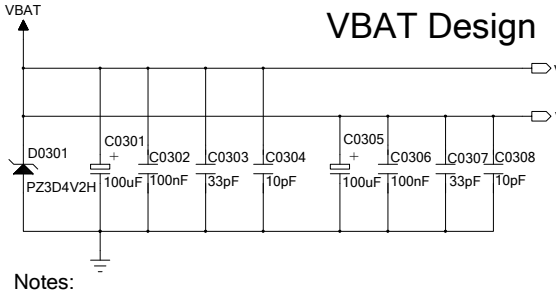


VBAT = (R0314/R0318+1)*1.24 = 3.3V

Notes:

1. The recommended load current of MIC29302WU is greater than 10mA.
2. The RC circuit, which is assembled with R0317 and C0327, is used to delay the start-up of MOSFET switch circuit.

VBAT Design

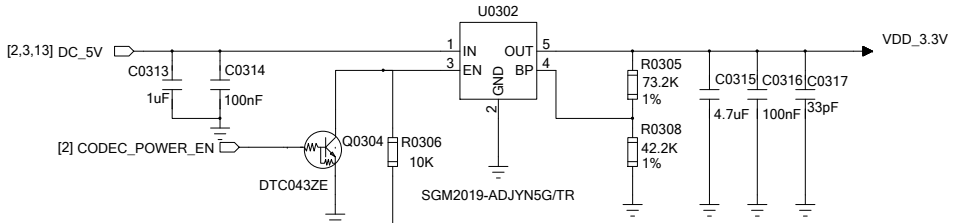


Notes:

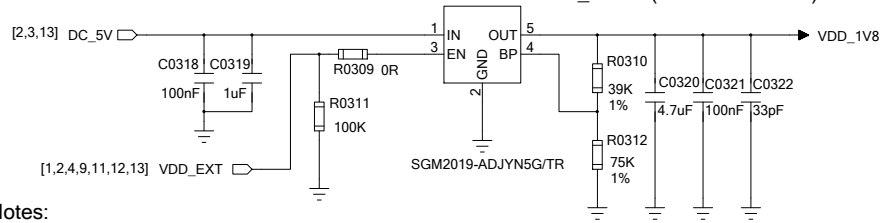
1. The power supply must be able to provide sufficient current up to 2A or more.
2. VBAT should be routed in star mode to VBAT_BB and VBAT_RF pins.
3. The recommended operating voltage of VBAT is 3.3V～4.3V.

Power Supply for PCM Codec

VDD_3.3V = (R0305/R0308+1)*1.207 = 3.3V



VDD_1V8 = (R0310/R0312+1)*1.207 = 1.8V



Notes:

1. CODEC_POWER_EN must be at low level in order to ensure the normal output voltage of VDD_3.3V. If VDD_3.3V power supply needs to be switched off, please keep CODEC_POWER_EN at high level.
2. The following power-on/off sequences should be complied with to ensure the audio codec works normally.
   Power-on Sequence: power on VDD_1V8 first, then VDD_3.3V.
   Power-off Sequence: power off VDD_3.3V first, then VDD_1V8.

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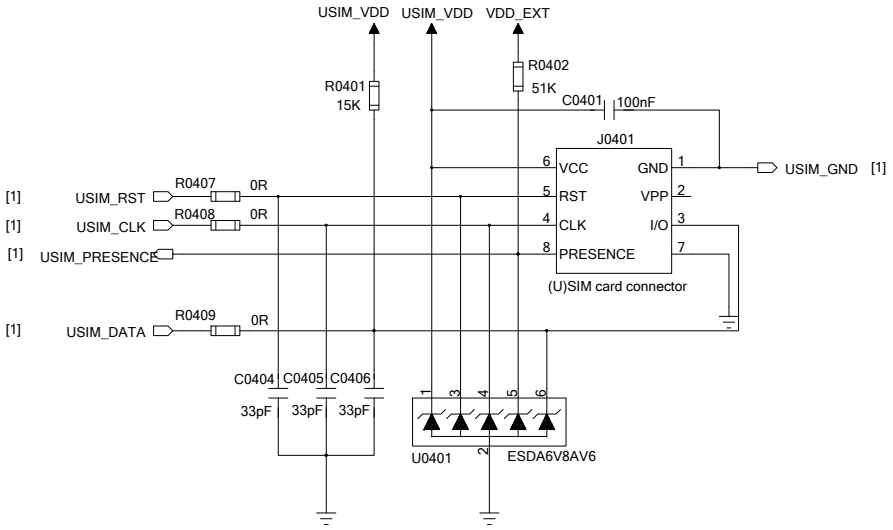
(U)SIM and UART Designs

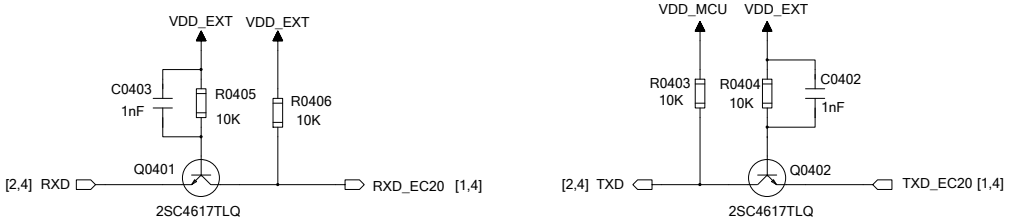
(U)SIM Interface



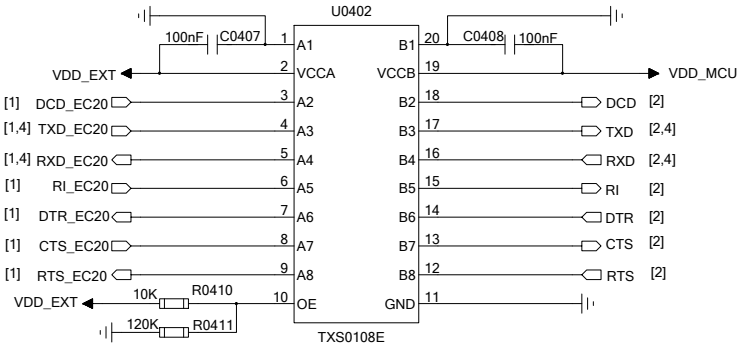
Notes:

1. U401 is recommended to be used to offer good ESD protection, and the parasitic capacitance should not be more than 15pF.
2. It is recommended to connect the (U)SIM card connector GND to the module USIM_GND. If the customer PCB GND is complete, it can be connected to the customer PCB GND directly.
3. The pull-up resistor R0401 can improve anti-jamming capability, and should be placed close to the (U)SIM card connector.
4. R0407～R0409 are used for debugging, C0404～C0406 are used for filtering interference of GSM900MHz.
5. C0401 capacitance should be less than 1uF, and should be placed close to the (U)SIM card connector.
6. For more information about the layout, please refer to *Quectel_EC20_R2.1_Hardware_Design*.

UART Translation - Transistor Solution



UART Translation - IC Solution



Notes:

1. There are two translation solutions: transistor solution and IC solution, and it is recommended to select the IC solution.
2. The power supply of VCCA should not exceed that of VCCB. For more information about TXS0108E, please refer to the datasheet from TI.
3. The transistor circuit solution is not suitable for applications with high baud rates exceeding 460Kbps. The 1nF capacitors C0402 and C0403 can improve the signal quality.
4. The RTS and DTR transistor circuits are similar to that of RXD interface. The CTS, RI and DCD transistor circuits are similar to that of TXD interface.

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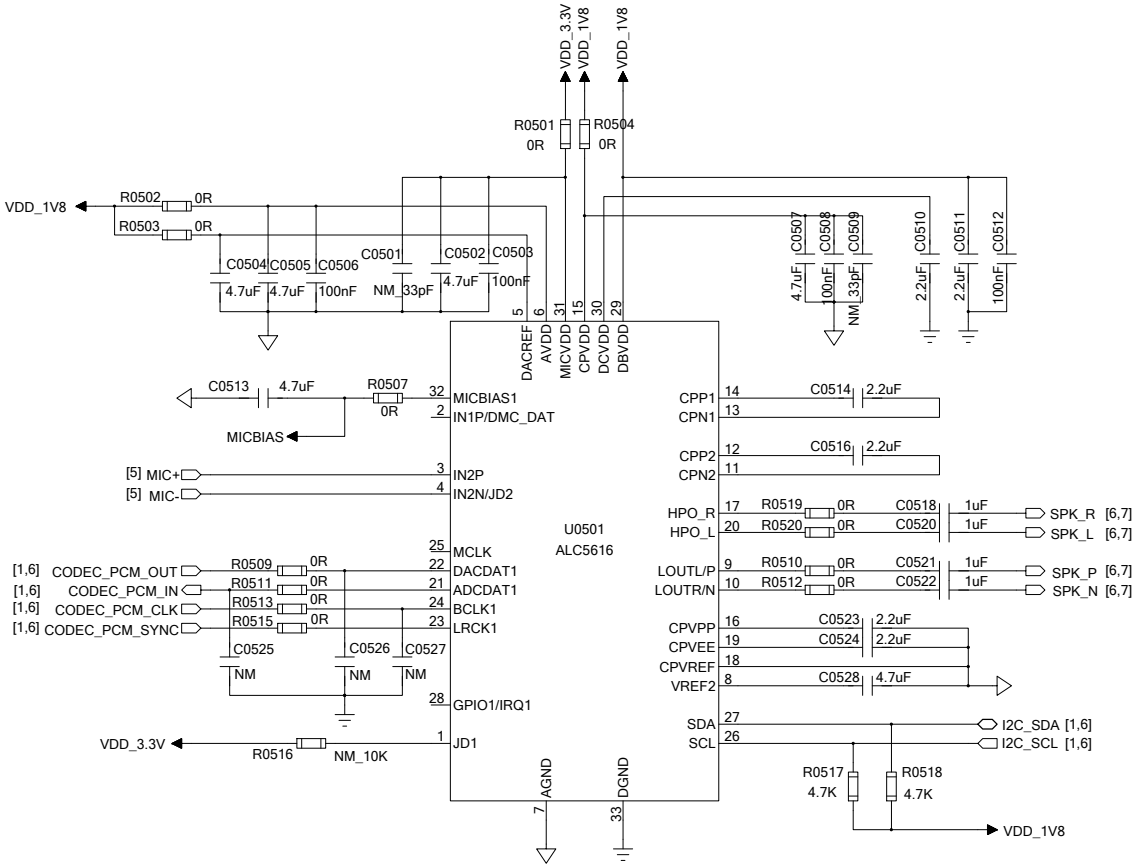
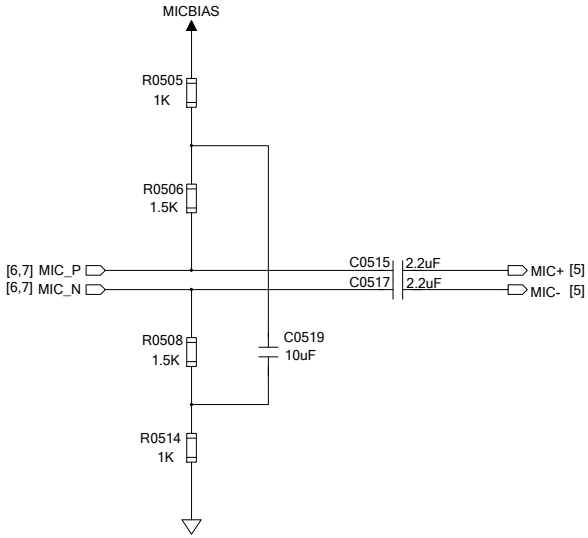
Audio Codec Design (ALC5616)





Notes:

1. ALC5616 power-on sequence: DBVDD/I2C pull-up power/AVDD/DACREF/CPVDD -> MICVDD -> software initialization.
2. ALC5616 power-off sequence: close codec function by software-> MICVDD -> DBVDD/I2C pull-up power/AVDD/DACREF/CPVDD.
3. EC20 R2.1 module will automatically initialize the codec via I2C interface after it is turned on successfully, so all power supplies for the codec need to be powered on before that.

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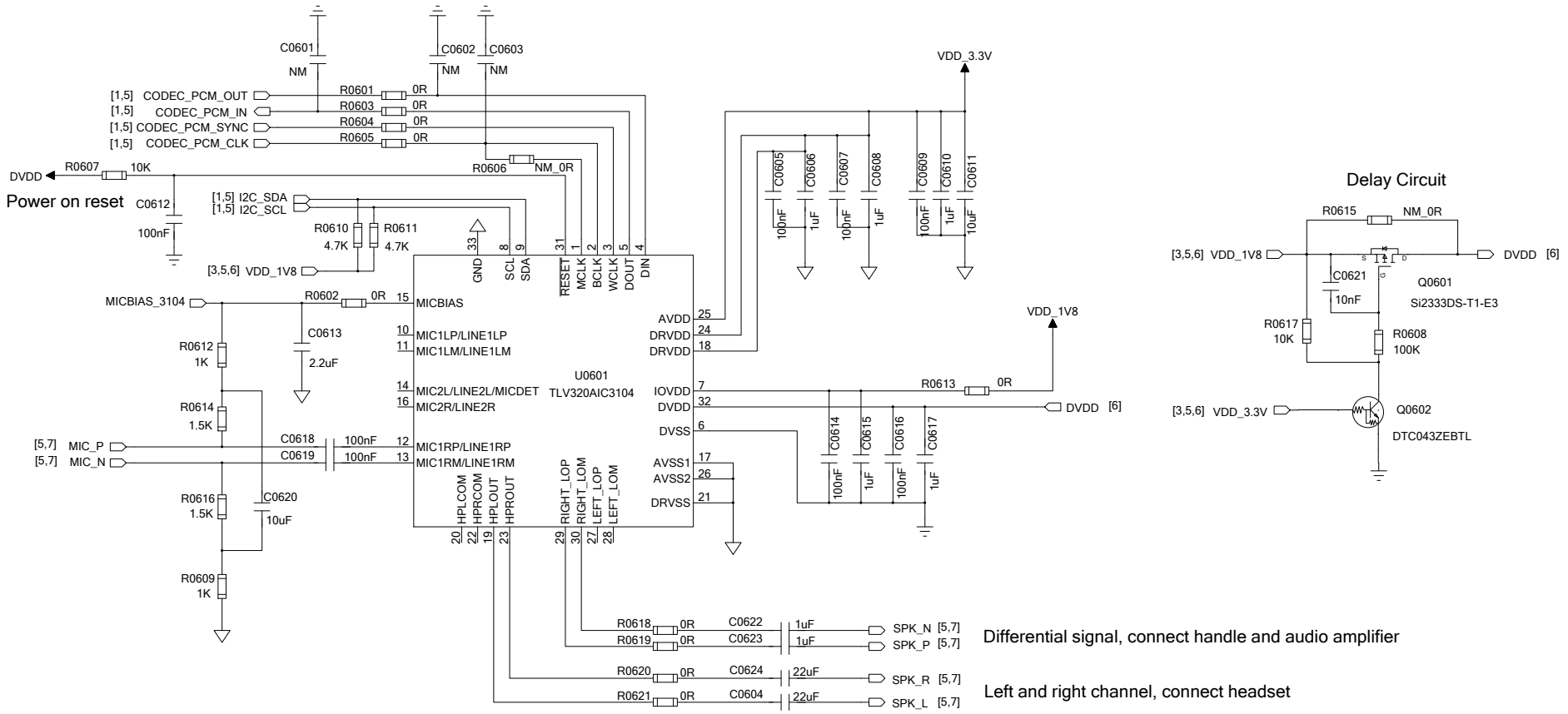
Audio Codec Design (TLV320AIC3104)



Differential signal, connect handle and audio amplifier

Left and right channel, connect headset

Notes:

1. TLV320AIC3104 power-on sequence: IOVDD -> AVDD/DRVDD -> DVDD -> software initialization.
2. The RC delay circuit, which is assembled with C0621 and R0608, is used to ensure that the power-on time difference between AVDD and DVDD is within 5ms.
3. The RESET pin must be driven at low level for at least 10ns after all power supplies for TLV320AIC3104 are at their specified values.
4. EC20 R2.1 module will automatically initialize the codec via I2C interface after it is turned on successfully, so all power supplies for the codec need to be powered on before that.

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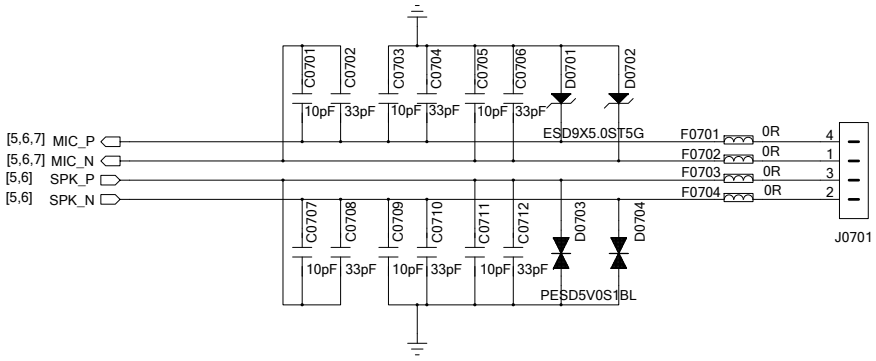
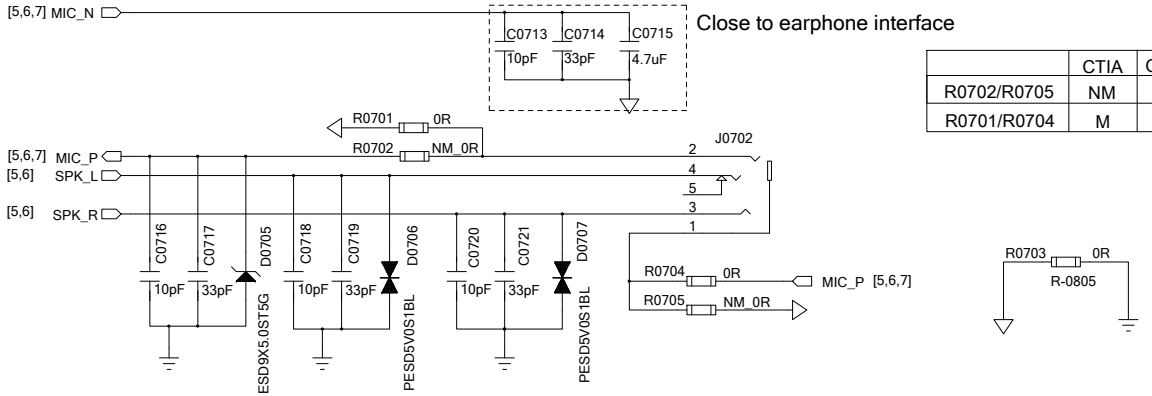
Audio Interface

Handset Application



Earphone Application



	CTIA	OMTP
R0702/R0705	NM	M
R0701/R0704	M	NM

Notes:

1. The analog output only drives earphone and headset. For larger power loads such as speakers, an audio power amplifier should be added in the design.
2. In handset application, both the MIC and SPK signal traces need to be routed as differential pairs.
3. In earphone application, the MIC signal traces need to be routed as differential pairs.
4. All MIC and SPK signal traces should be routed with total grounding and far away from noise such as clock and DC-DC signals, etc.
5. ALC5616 and TLV320AIC3104 cannot be used simultaneously in audio codec design.

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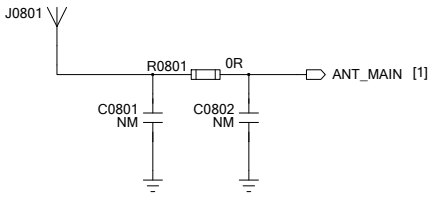
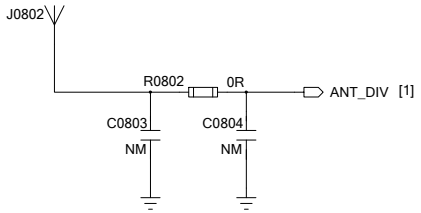
RF and GNSS Designs

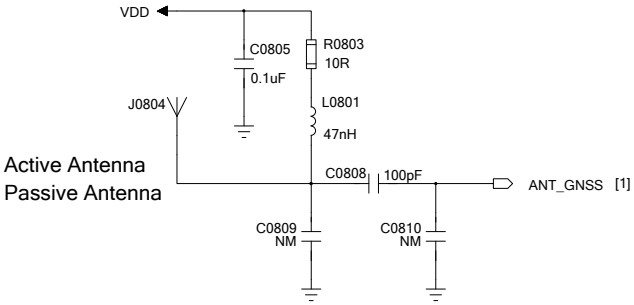
Main Antenna Circuit



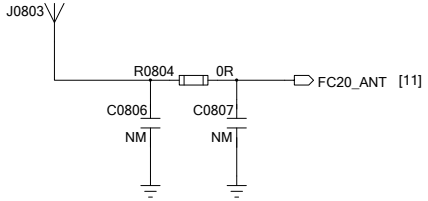
Diversity Antenna Circuit



GNSS Antenna Circuit



FC20 Antenna Circuit



Notes:

1. It is recommended to use PI type main/Rx-diversity/FC20 antenna circuit, thus ensuring convenient subsequent debugging.
2. The diversity reception function is ON by default. If diversity antenna is not used, there is a need to use AT command to turn off diversity reception.
3. An external LDO can be selected to supply power for active antenna.
4. If passive antenna is used, then R0803 and L0801 are not needed.
5. The impedance of the RF signal traces must be controlled as 50Ω when routing.

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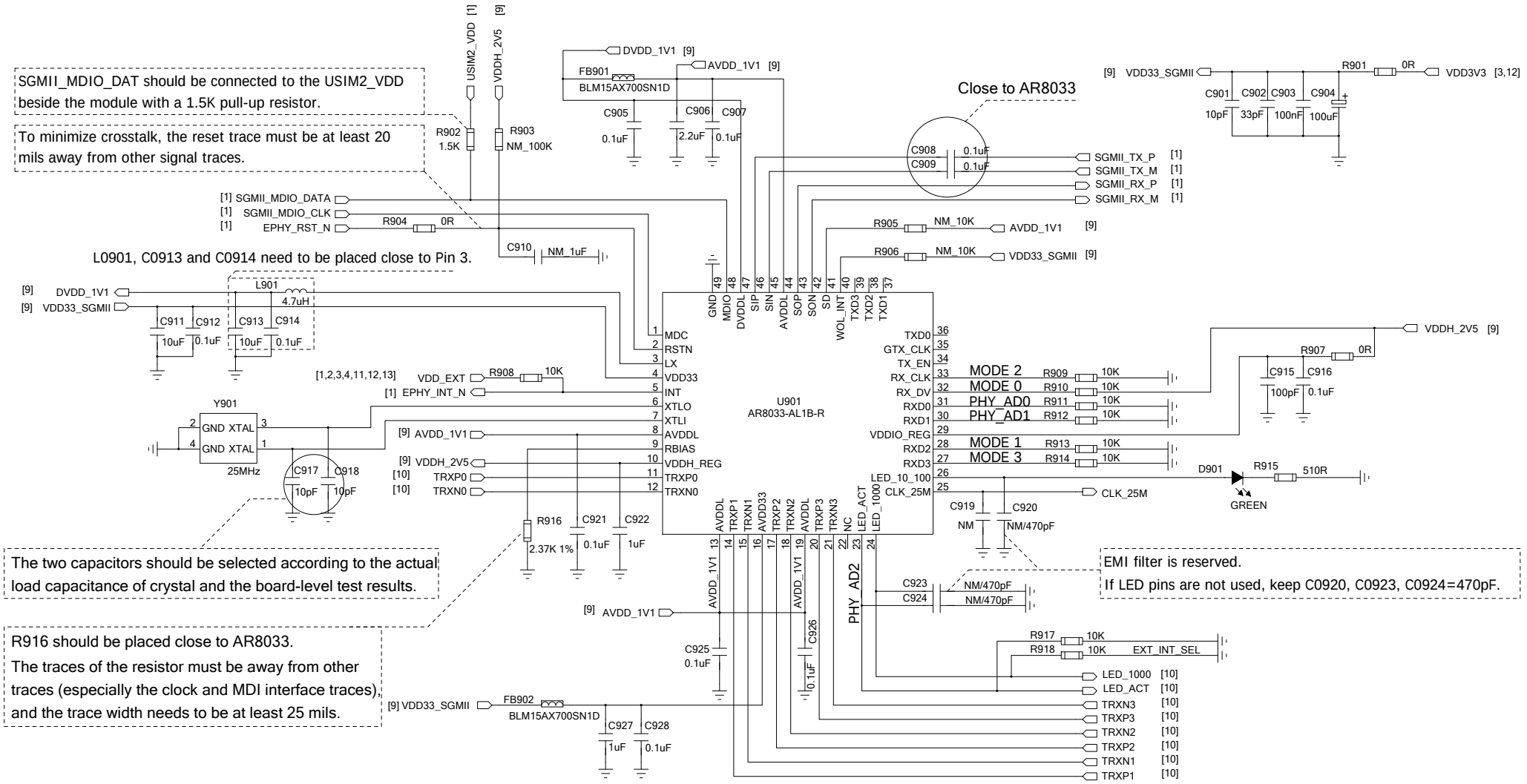
Ethernet PHY Design



Notes:

1. In the following description, the SGMII data signal refers to the SGMII TX and RX difference pair, and the SGMII control signal refers to the SGMII_MDIO_CLK, SGMII_MDIO_DATA, EPHY_RST_N and EPHY_INT_N.
2. SGMII data and control signals should be strictly protected with ground and kept away from RF, analog, clock and DCDC signals etc.
3. Keep the maximum trace length of SGMII data signal less than 10-inch and keep skew of the TX and RX signals less than 20mil.
4. The differential impedance of SGMII data signal is 100Ω±10%, and the reference ground of the area should be complete.
5. Make sure the trace spacing between SGMII RX and TX is at least 3 times of the trace width, and the same to the adjacent signal traces.
6. The peripheral circuit layout of Ethernet PHY chip AR8033 should be designed on a four-layer PCB, and the second layer should be total grounded as the AR8033 reference GND.
7. RJ45, network transformer, AR8033, and the SGMII interface should be placed close to each other.

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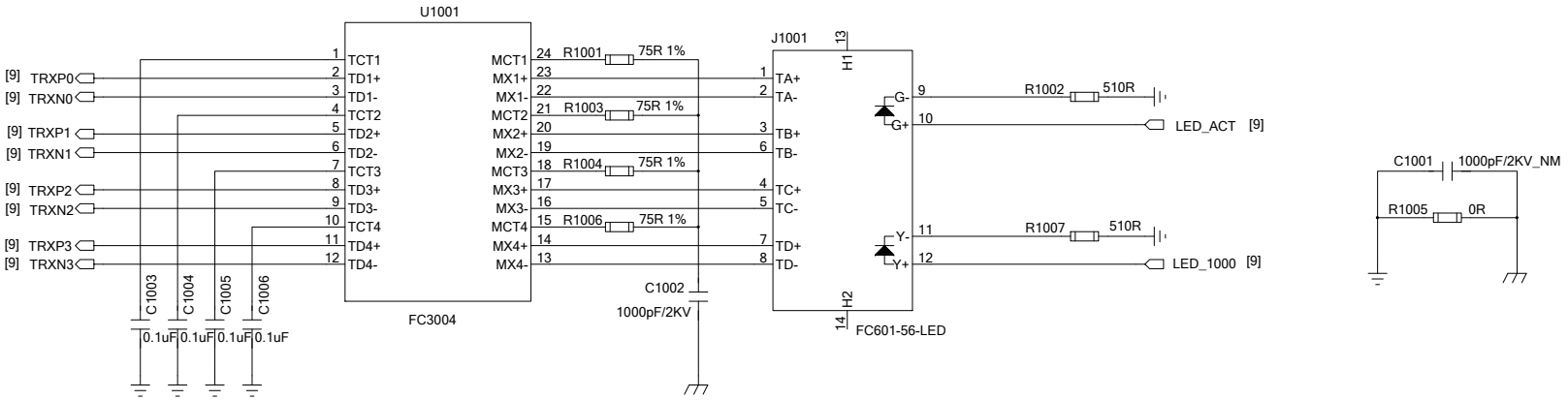
Ethernet Network Port Design



PHY core configuration signal	Description	Default internal weak pull-up/down	Application external weak pull-up/down
PHY_AD2	PHY_AD[2:0] set the lower three bits of the physical address. The upper two bits of the physical address are set to 00.	1	0
PHY_AD1		0	0
PHY_AD0		0	0
MODE 3	Mode select bit 3	0	0
MODE 2	Mode select bit 2	0	0
MODE 1	Mode select bit 1	0	0
MODE 0	Mode select bit 0	0	1
EXT_INT_SEL	An external 10K pull-down resistor is required.	1	0
0 = Pull-down, 1 = Pull-up.			

Notes:

1. Route MDI differential signals with 100Ω±10%, and the reference ground of the area should be complete.
2. Keep skew of the MDI differential signals less than 20mils, and the maximum trace length must be less than10 inches.
3. To minimize crosstalk, the distance between separate adjacent pairs that are on the same layer must be equal to or larger than 40 mils.

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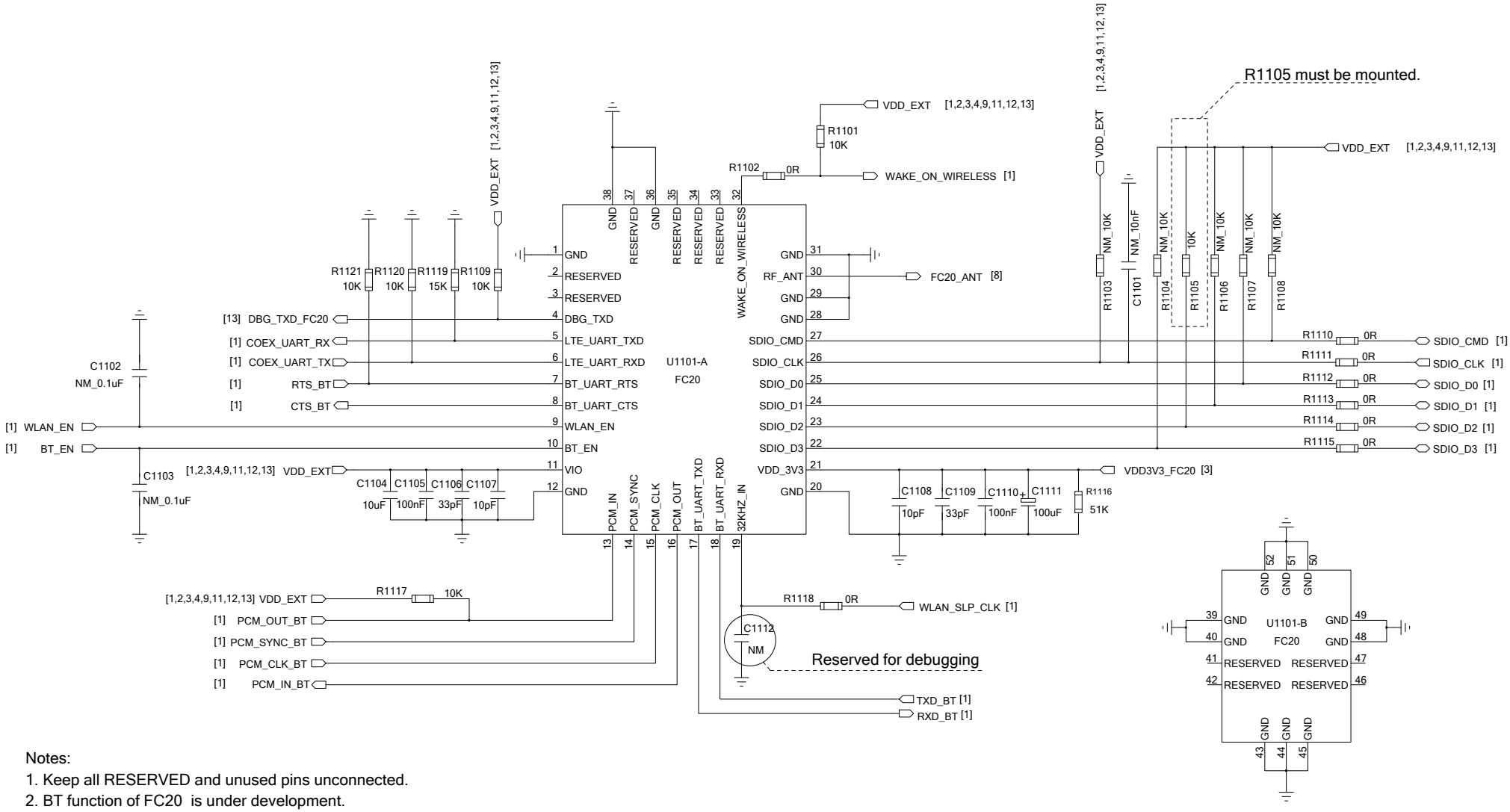
FC20 Design



Notes:

1. Keep all RESERVED and unused pins unconnected.
2. BT function of FC20 is under development.
3. Keep SDIO signals far away from other sensitive circuits/signals such as RF circuits, analog signals, etc, as well as noisy signals such as clock and DC-DC signals, etc.
4. Route SDIO signals with 50Ω±10% impedance. It is important to route the SDIO signal traces with total grounding, and the total routing length should be less than 50mm.
5. It is recommended to keep the matching length between CLK and DATA/CMD less than 1mm.
6. Make sure the adjacent trace spacing is two times of the trace width and the bus capacitance is less than 15pF.
7. The pins 5～8, 10, 13～18 should be unconnected when using FC20-N.
8. FC20 power-on sequence: VIO -> VDD_3V3.

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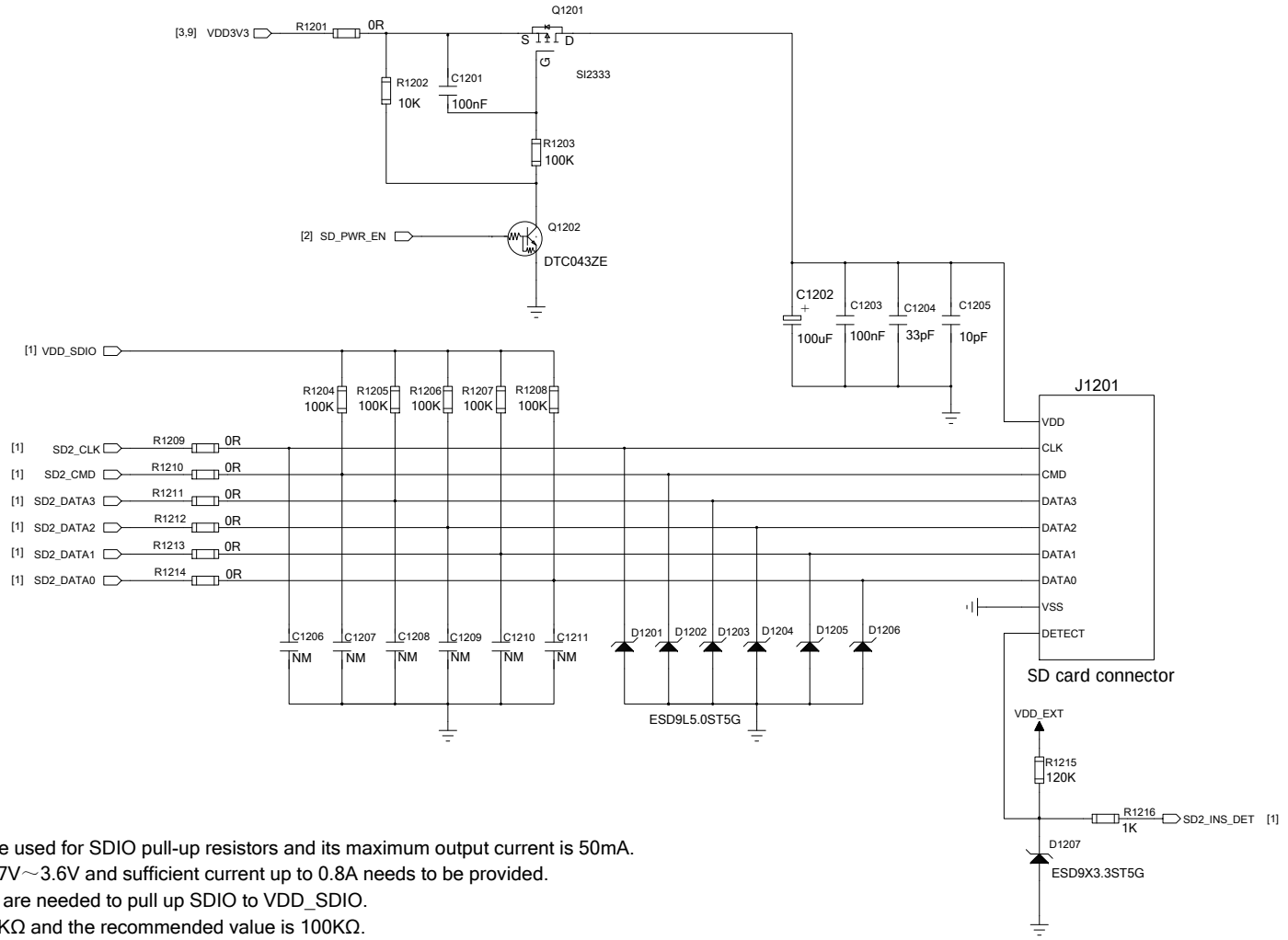
SD Card Interface Design



Notes:

1. The pin 34 (VDD_SDIO) on the module can only be used for SDIO pull-up resistors and its maximum output current is 50mA.
2. The supply voltage range of VDD for SD card is 2.7V～3.6V and sufficient current up to 0.8A needs to be provided.
3. To avoid the jitter of bus, resistors R1204～R1208 are needed to pull up SDIO to VDD_SDIO.
   The value of these resistors is among 10KΩ～100KΩ and the recommended value is 100KΩ.
4. In order to adjust signal quality, it is recommended to add 0Ω resistors R1209～R1214 in series between the module and the SD card connector.
   The bypass capacitors C1206～C1211 are reserved and not mounted by default.
5. It is recommended to add ESD protection devices near the pins of SD card connector. The parasitic capacitance of ESD protection devices should be smaller than 15pF.
6. Keep SDIO signals far away from other sensitive circuits/signals such as RF circuits, analog signals, etc, as well as noisy signals such as clock and DC-DC signals, etc.
7. Route SDIO signals with 50Ω±10% impedance. It is important to route SDIO signals with total grounding, and the total trace length should be less than 23mm.
8. It is recommended to keep the trace length difference between CLK and DATA/CMD less than 1mm.
9. Make sure the adjacent trace spacing is two times of the trace width and the bus capacitance is less than 15pF.

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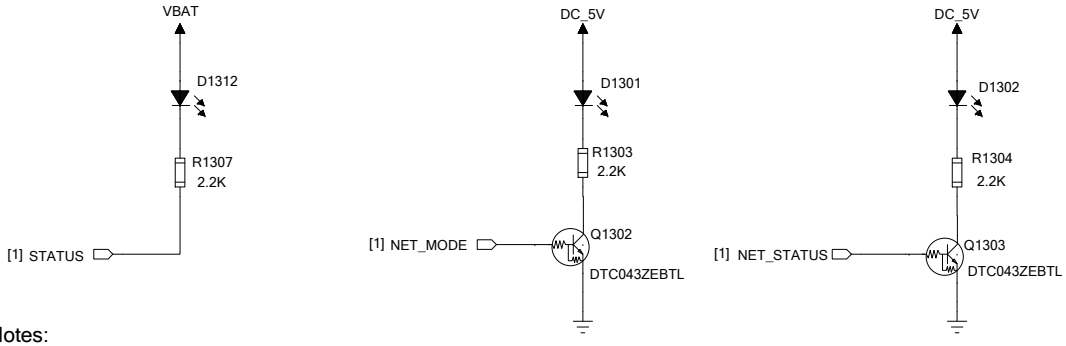
Other Designs

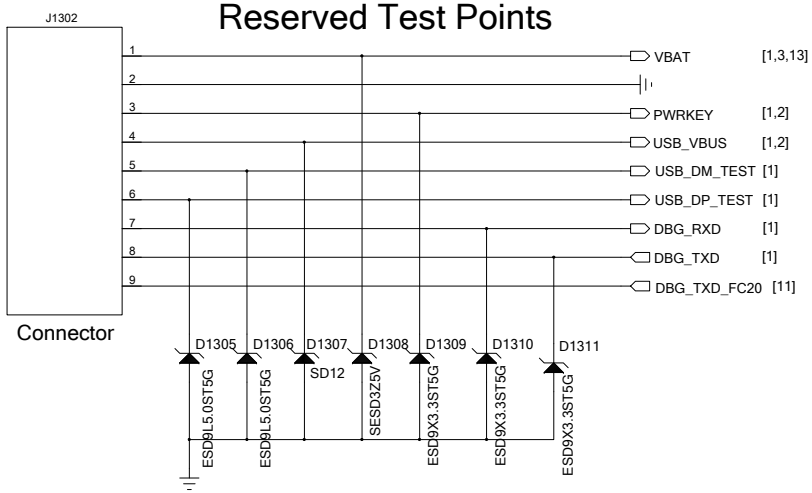
Indicators



Notes:

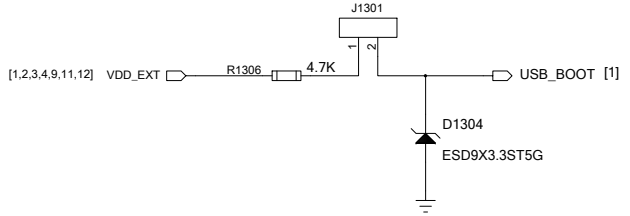
1. The STATUS is an open drain output pin, and its drive current is less than 1mA.
2. For more details about NET_MODE and NET_STATUS, please refer to *Quectel_EC20_R2.1_Hardware_Design*.
3. If the current consumption is required as low as possible when the device is in sleep, replace the power supply of indicators with controllable one.
   Turn off the power when the module enters into sleep mode.

Reserved Test Points



Notes:

1. Both USB and debug UART interfaces are reserved for software debugging.
2. USB interface also can be used to upgrade firmware.
3. Junction capacitance of ESD protection devices on USB data lines should be less than 1pF.
4. The module DBG interface supports 1.8V power domain,
   A level translator should be used if the power domain of customers' application is 3.3V.



Notes:

1. It is recommended to reserve USB_BOOT design.
2. USB_BOOT is kept open by default.
   When it is at high level, the module will enter download mode.

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