BG95 Series&BG96

PCB Design Guidelines

LPWA Module Series

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Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any cellular terminal or mobile incorporating the module. Manufacturers of the cellular terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for customers' failure to comply with these precautions.

	Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the cellular terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.
	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.
	Cellular terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergency help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the cellular terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.
	The cellular terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.
	In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other cellular terminals. Areas with explosive or potentially explosive atmospheres include fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.

About the Document

Revision History

Version	Date	Author	Description
-	2020-12-11	Tanveer Hussain	Creation of the document
1.0	2021-01-15	Tanveer Hussain	First official release

Contents

Table Index

Figure Index

1 Introduction

The layout of printed circuit board (PCB) is an important step in maintaining the high performance of the device. This document mainly introduces the PCB design guidelines for BG95 series and BG96 modules, and it takes BG95-M3-TE-A, ALC5616-TE-A and UMTS&LTE EVB as examples.

This document is applicable to the following modules:

- BG95 series
- BG96

2 PCB Design Overview

2.1. Footprint

Check out the module's footprint and pay attention to the following points.

- First, check whether the module's footprint is of the latest version provided by Quectel. Is the number of pins correct? Are the pin distribution position and pin definition being both correct? For specific footprint of the module, see ***document [1]***.
- The recommended number of PCB layers is 4 or more. If there are few functions and the cost is strict, 2-layer boards can be considered.

2.2. Design Priorities

1. Antenna traces.
2. High-speed signal USB traces.
3. Power supply (VBAT_BB, VBAT_RF, USIM_VDD, PWRKEY and RESET_N) traces.

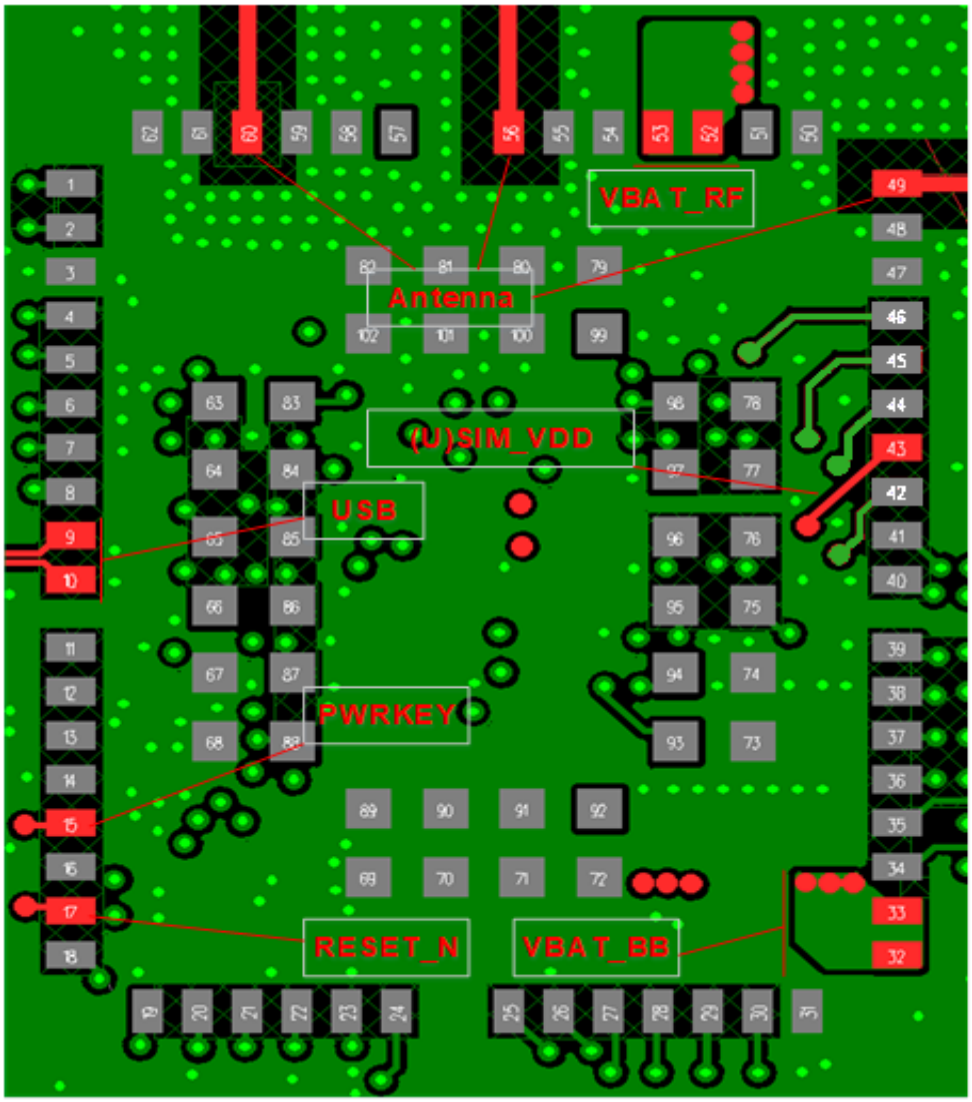

Figure 1: Interfaces with Higher Priorities (TE-A 1st Layer)

3 Interface Design

3.1. Power Supply

3.1.1. DC-DC Converter

- The DC-DC converter should be away from the sensitive signal traces such as USB, audio, RF, (U)SIM and CLK.
- The input/output capacitors and the inductor should be placed as close as possible to the IC. This keeps the power traces short. Routing the power traces directly and widely results in low trace resistance and low parasitic inductance.
- The low side of the input and output capacitors must be connected to the power GND properly to avoid a potential ground shift problem.

Refer to the figures below as an example.

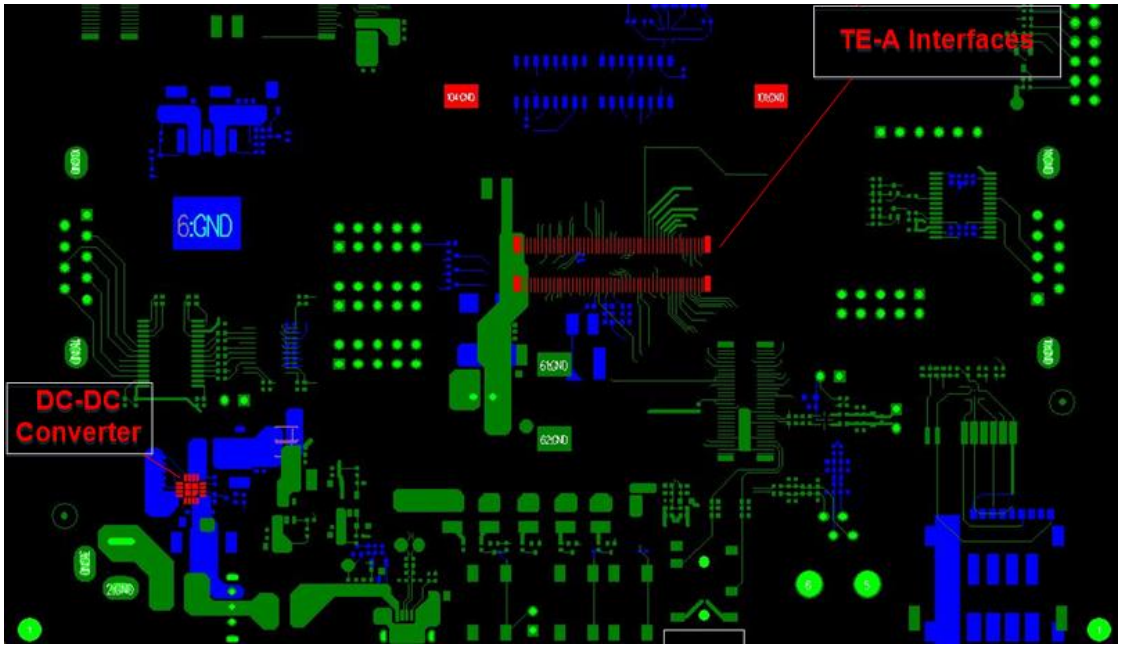

Figure 2: DC-DC Converter (EVB 4th Layer) and TE-A Interfaces (EVB 1st Layer)

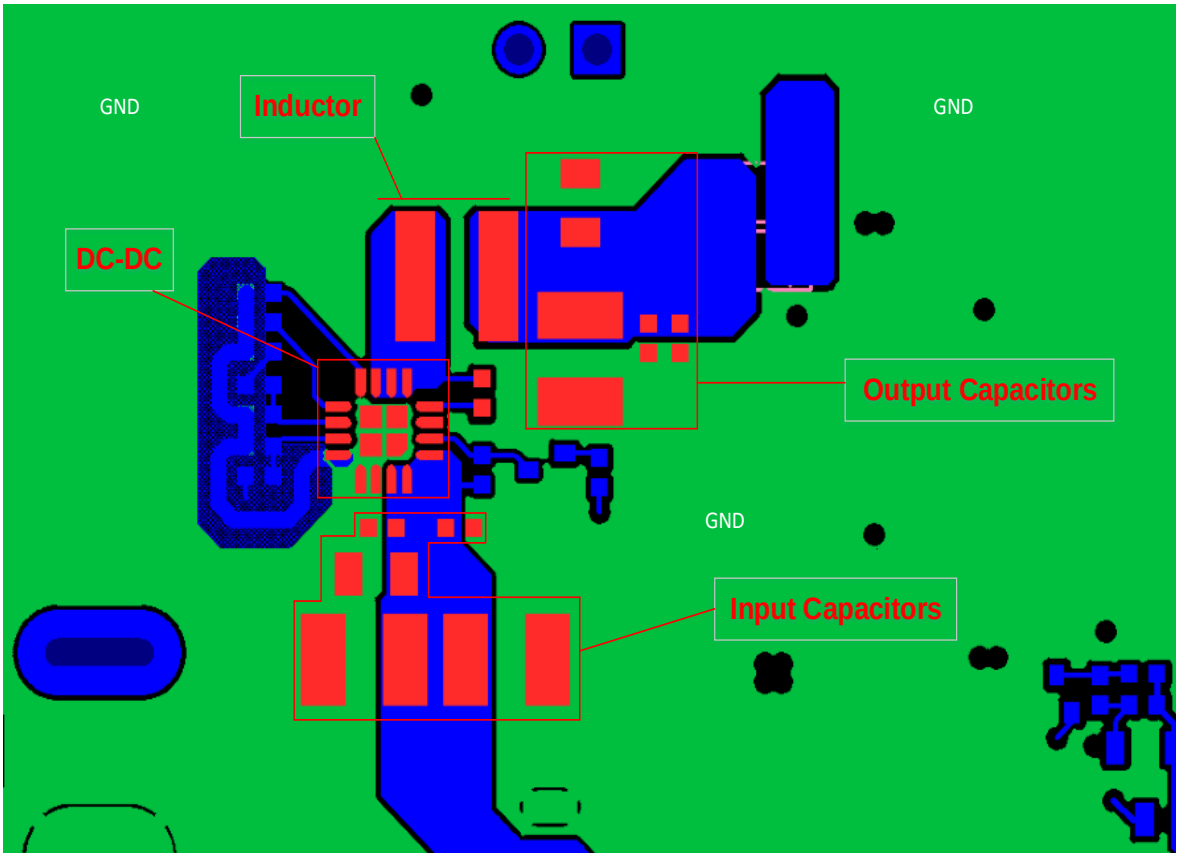

Figure 3: Capacitors and Ground Surrounding of DC-DC Converter (EVB 4th Layer)

3.1.2. VBAT

- Place 10 pF, 33 pF, 100 nF and 100 μF capacitors for both VBAT_BB and VBAT_RF. The filter capacitors and TVS diodes on VBAT circuit should be placed as close to the module as possible. The smaller the capacitor value is, the closer it is to the module pin.

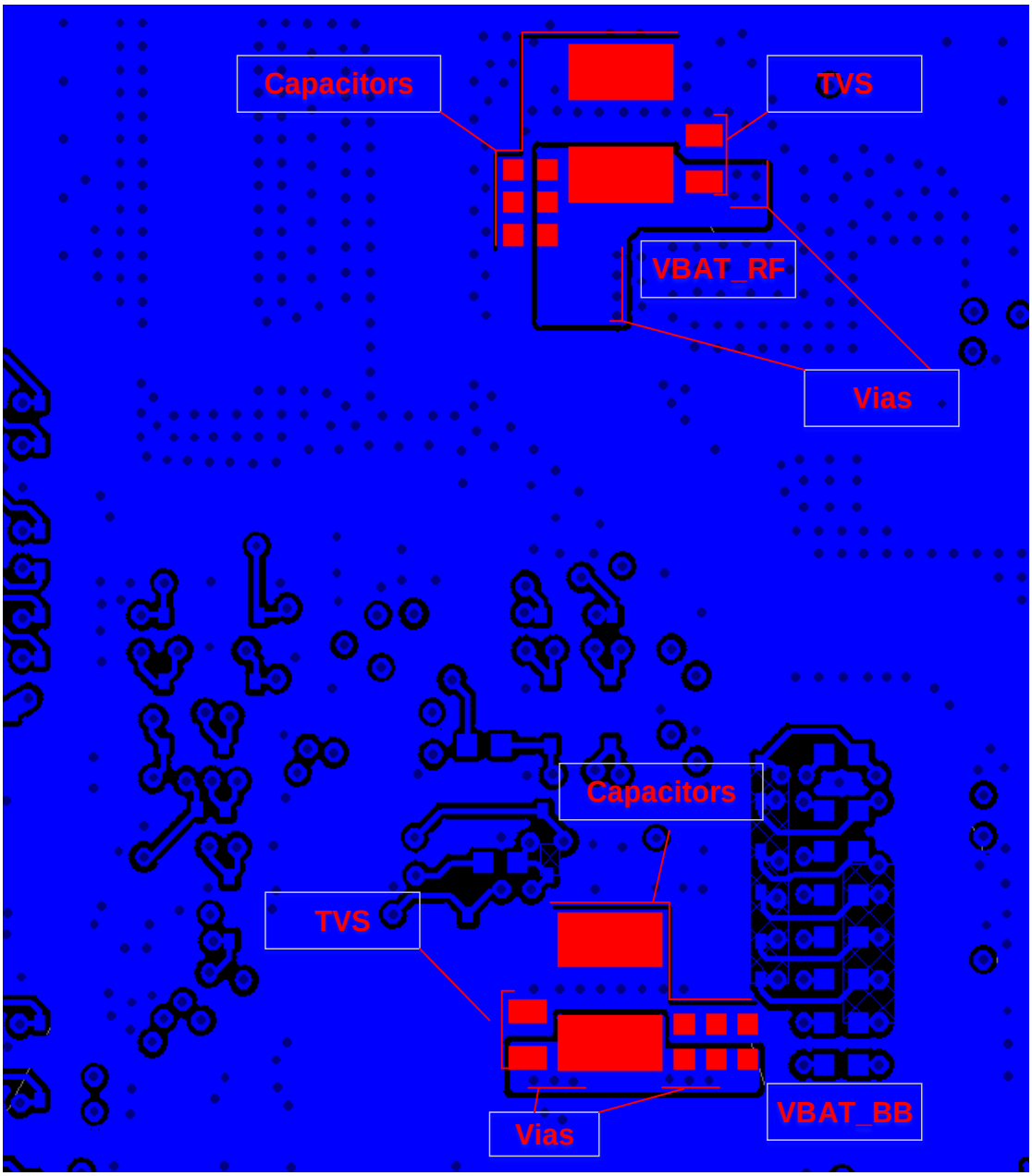

Figure 4: VBAT Capacitors and TVS Diodes (TE-A 4th Layer)

- VBAT_BB trace width: > 0.6 mm, with at least 5 vias; VBAT_RF trace width: > 2 mm, with at least 6 vias. In principle, the longer the VBAT trace, the wider it should be.
- Keep VBAT traces away from sensitive signal traces such as USB, audio, RF, CLK and I2C. Avoid crossing or paralleling the VBAT traces with those sensitive signal traces.
- It is recommended that VBAT_BB and VBAT_RF are designed as star connection. Avoid daisy chaining section grounds where the ground from one section feeds the next, and daisy chaining would cause each successive section to inherit ground noise from the previous section.

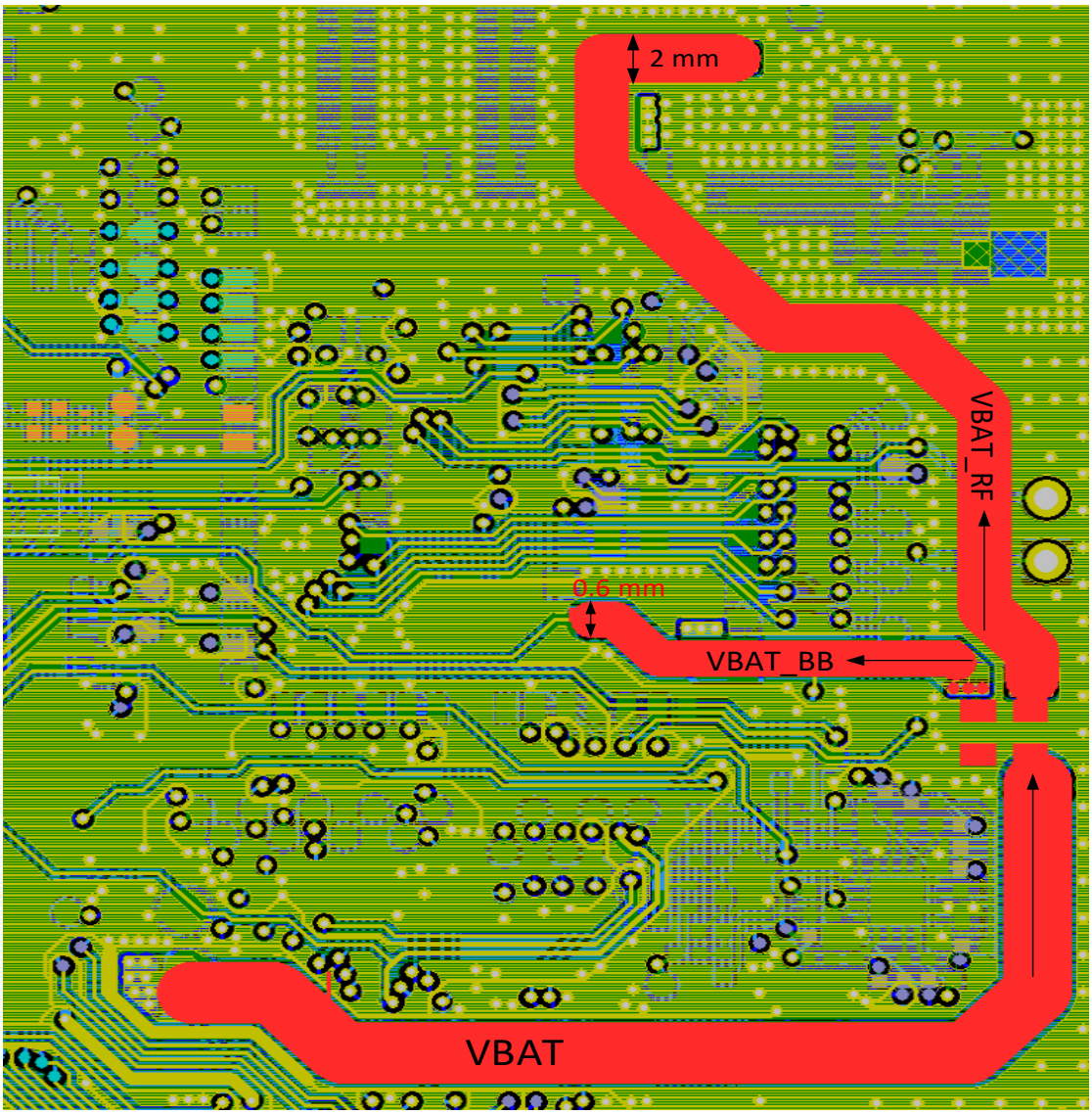

Figure 5: VBAT Star Connection (TE-A Multi Layers)

3.1.3. PWRKEY & RESET_N

- PWRKEY and RESET_N signal traces should be ground surrounded.
- If filter capacitors for PWRKEY and RESET_N exist, put them near the two pins and ESD protection component near the keypad.

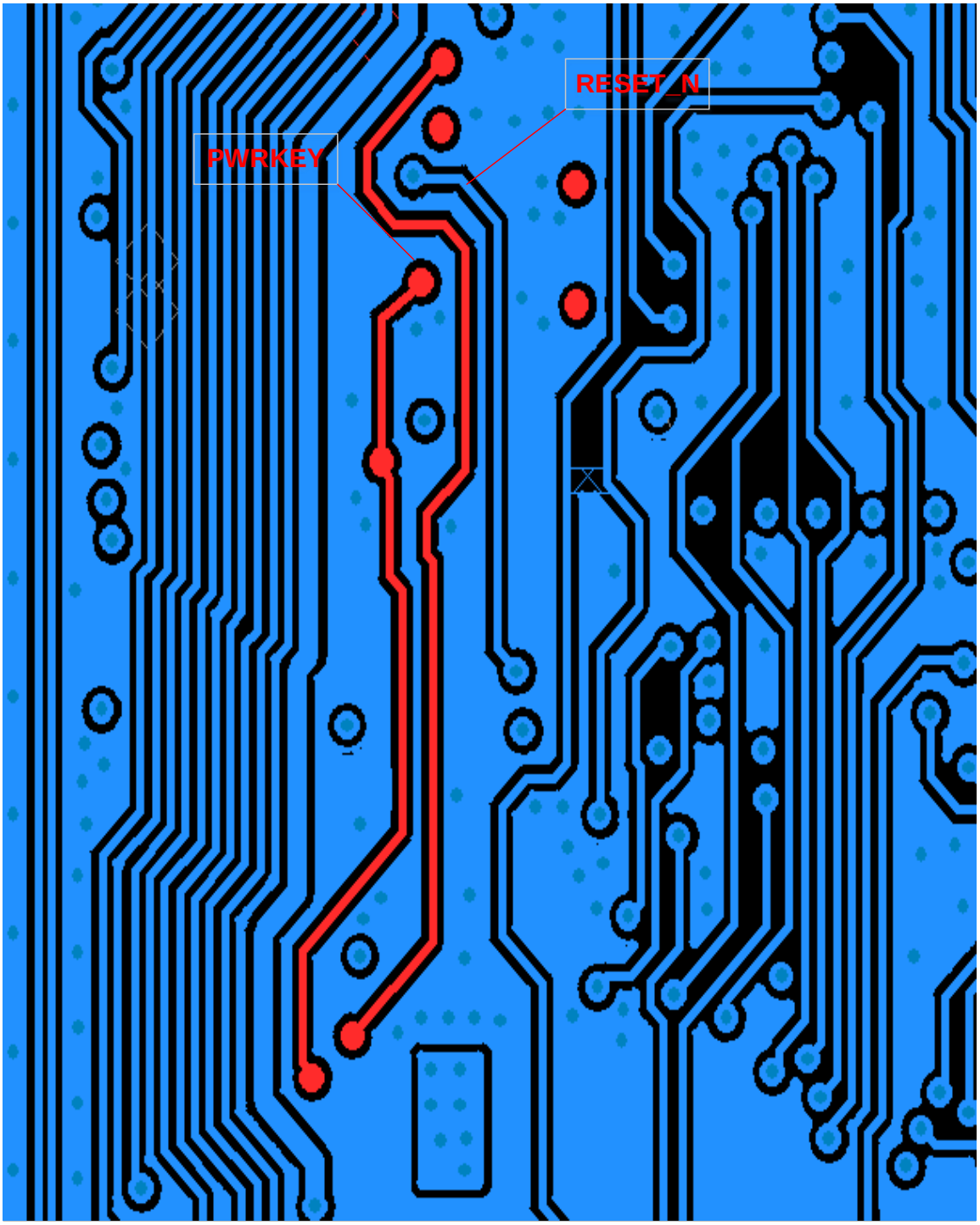

Figure 6: PWRKEY and RESET_N Traces (TE-A 3rd Layer)

3.2. USB Interface

3.2.1. USB_DM & USB_DP

- Make the length and width of USB_DM trace equal to that of USB_DP trace, and the difference between the lengths is no more than 2 mm for BG95 series and 3.8 mm for BG96. The total length of USB_DM or USB_DP trace should be no more than 200 mm for BG95 series and 150 mm for BG96. This trace length is different for each module.
- If the USB trace has a reserved test point, the stub of the test point should be as short as possible.
- It is suggested to route the USB signal traces in the middle layer of the board, surround the USB signal traces with ground and also keep them away from power supply and sensitive signal traces.
- Drill as few vias as possible for the USB interface as vias will affect the continuity of the impedance. And route the differential pair trace in the same layer.
- Place ESD protection components near the USB connector.
- Keep the impedance of 90 Ω for USB signal traces.

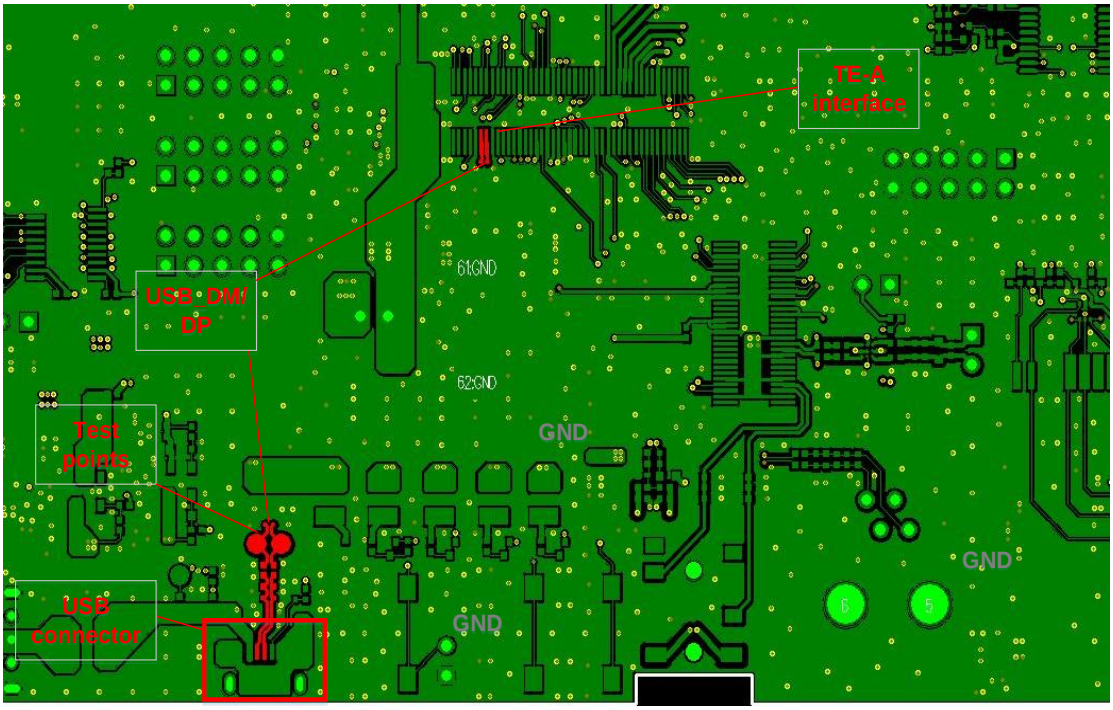

Figure 7: Overview of USB_DP/DM Signal Traces (EVB 1st Layer)

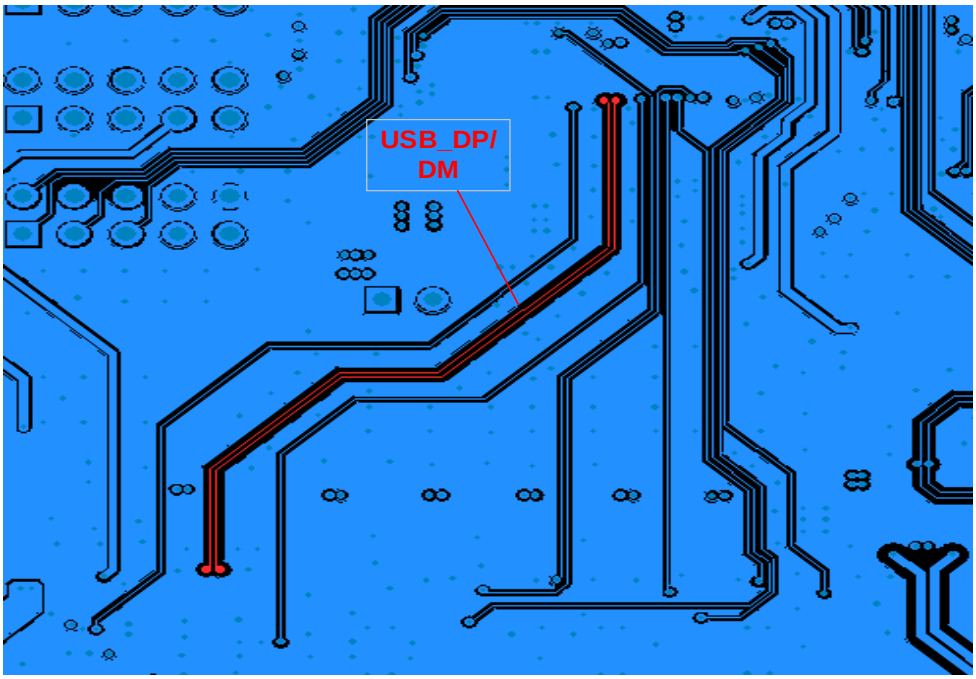

Figure 8: Overview of USB_DP/DM Signal Traces (EVB 3rd Layer)

3.2.2. USB_VBUS

USB_VBUS is the USB detect signal with a maximum current of 1 mA, so a trace width of 0.1 mm is enough.

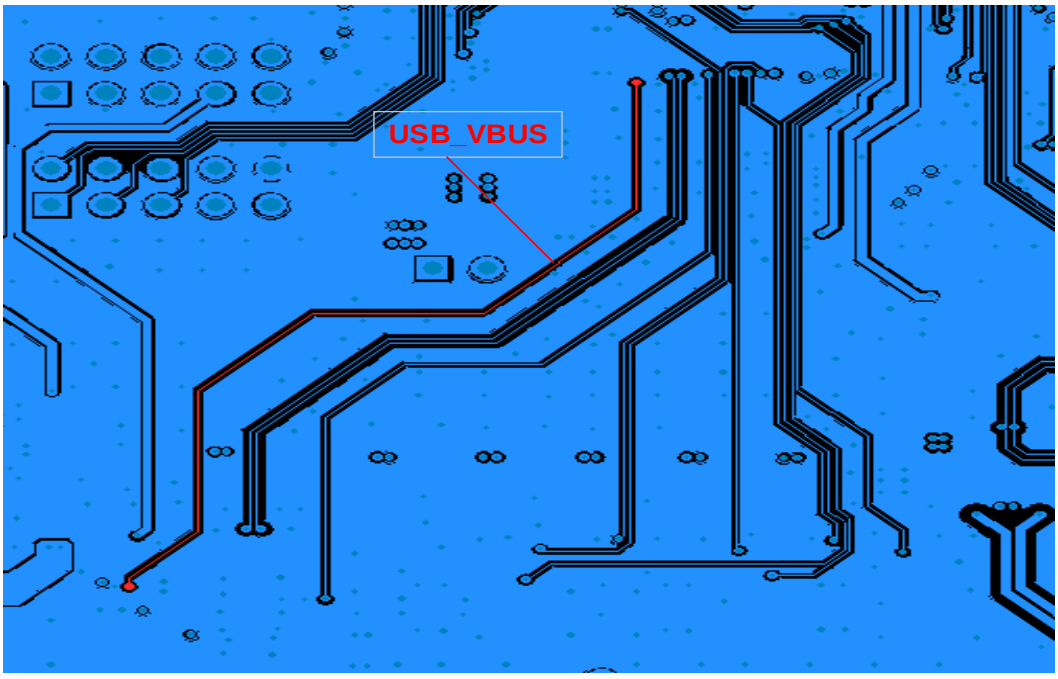

Figure 9: Overview of USB_VBUS Signal Trace (EVB 3rd Layer)

3.3. Debug UART Interface

If space is available, try to surround the UART traces with ground. If not, it can be considered that UART traces are not ground surrounded, but keep them away from the power supply and other interference sources.

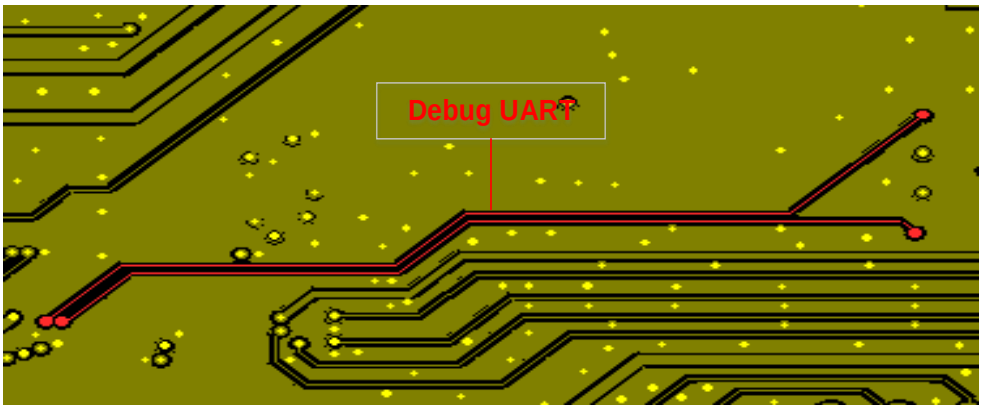

Figure 10: Debug UART Traces (EVB 2nd Layer)

3.4. Audio Interfaces

3.4.1. PCM Interface

- PCM signal traces should be away from those sources with interference such as RF, CLK, crystal and VBAT.
- It is recommended to route the PCM traces in the inner layer of the board and surround them with ground. If there is no limitation of space, surround the PCM_CLK with ground and route the other three signal traces together.
- It is suggested that the RC circuit is reserved for PCM_CLK signal.

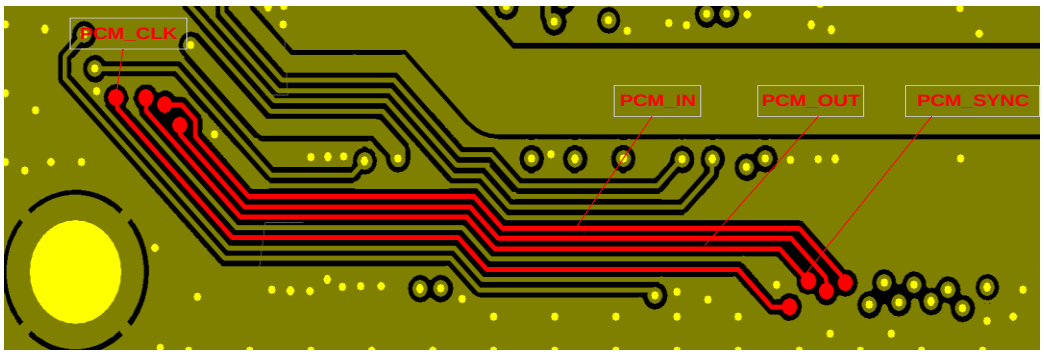

Figure 11: PCM Traces (TE-A 2nd Layer)

3.4.2. Codec, Microphone & Speaker

- Codec power supply is not recommended to take power from the VBAT pin. Keep codec signals away from VBAT, CPU, DRAM, Flash, PMU, LCD, RF antenna, etc. and surround them with ground if there is a space.
- In earphone application, route the MIC signal traces as differential pairs.
- Route all MIC and SPK signal traces with ground surrounded and far away from noise such as CLK and DC-DC signals.
- Route MIC and SPK traces as short as possible. MIC has a differential input. The space between MIC_P and MIC_N should be less than 10 mils. To avoid cross-talk, the space between 2 MICs should be more than 60 mils and should be located at different layers. Differential output is recommended for SPK, which requires low trace impedance and the trace width should be more than 20 mils.
- The reference ground for MIC, SPK and MICBIAS is recommended to be analog ground. AGND needs to be connected with DGND on a single point. DGND can also be used alone.
- The gap between AGND and DGND should be no less than 1 mm.

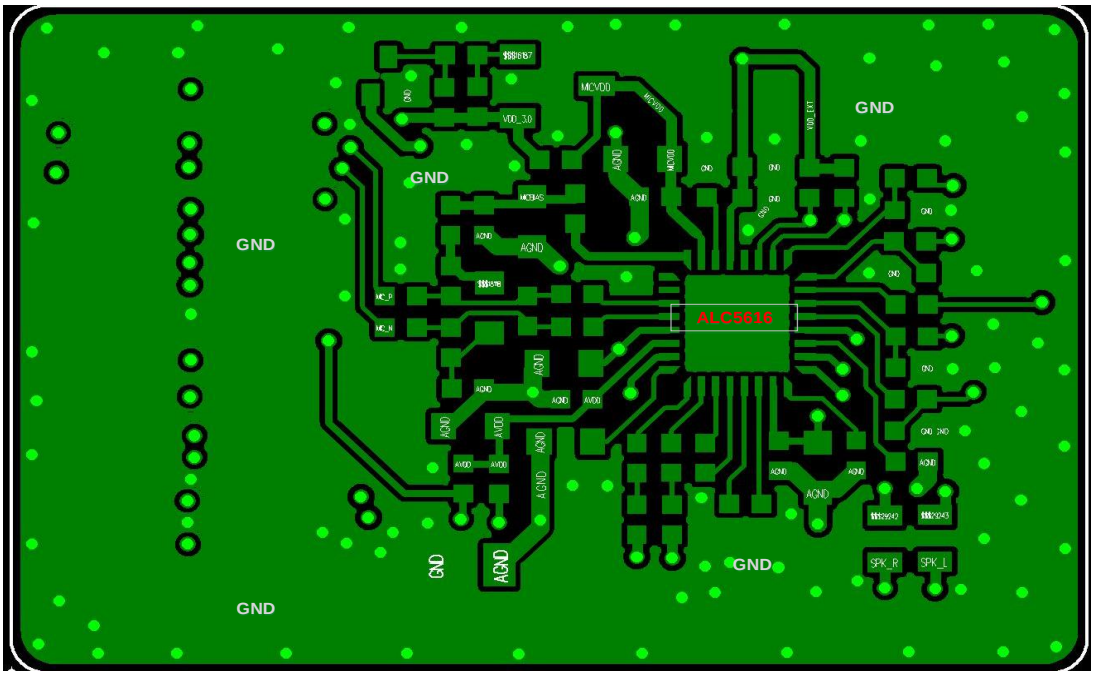

Figure 12: Overview of Codec ALC5616 (TE-A 1st Layer)

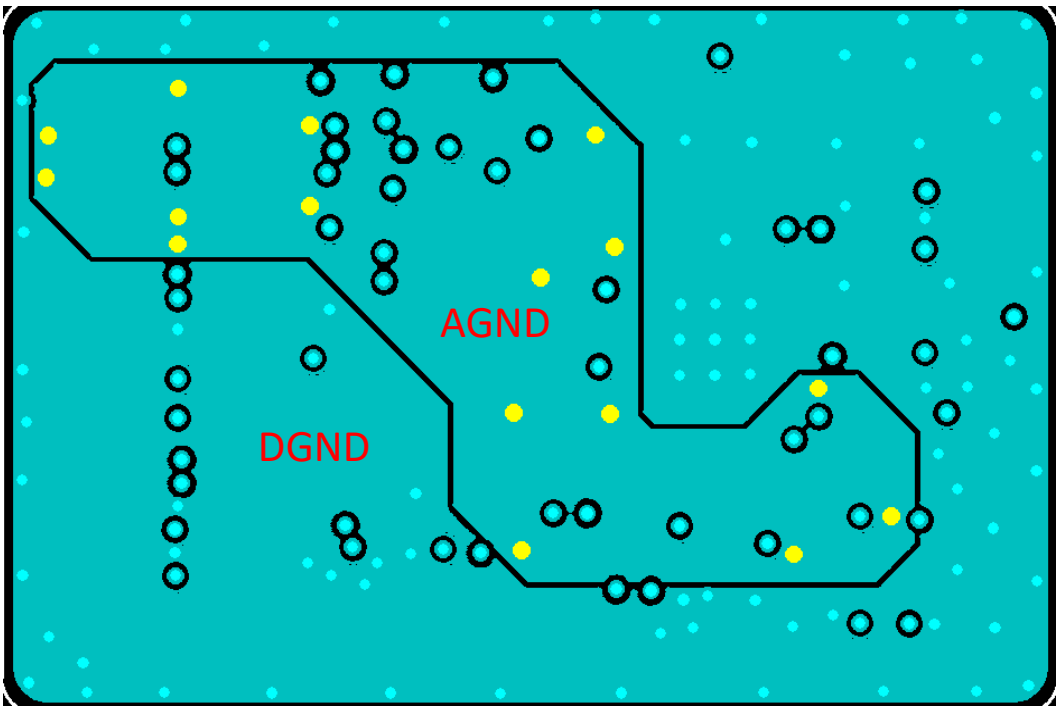

Figure 13: Overview of Codec ALC5616 AGND & DGND (EVB 2st Layer)

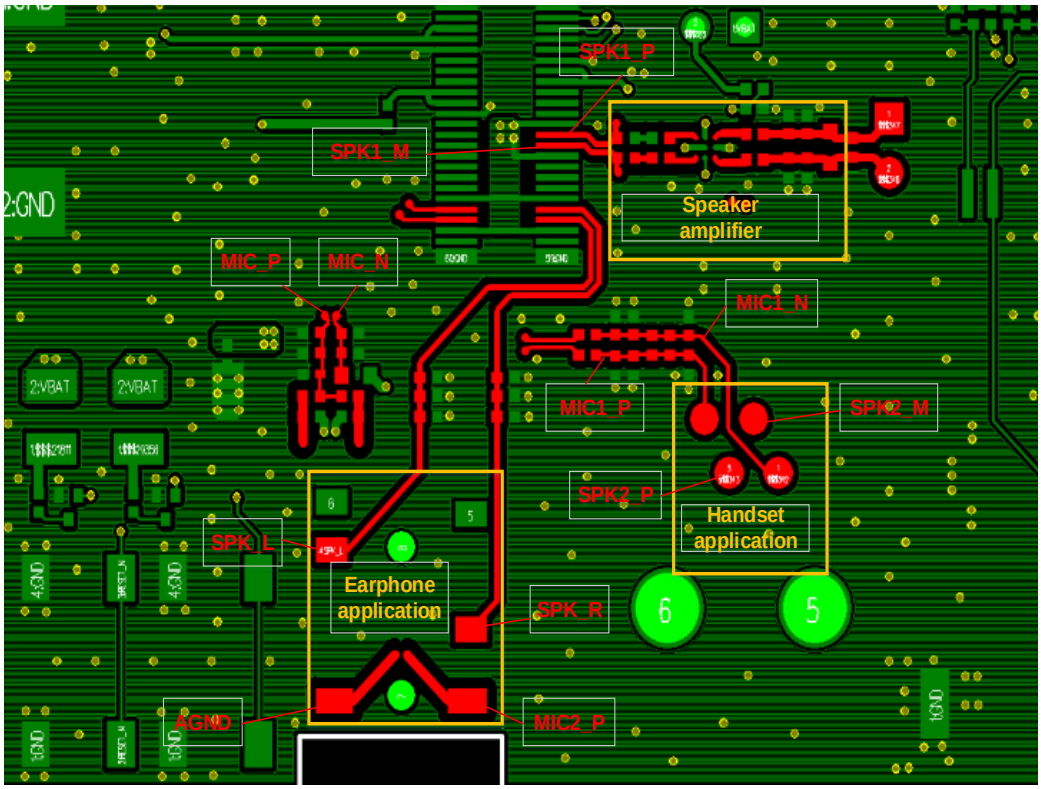

Figure 14: Overview of Analog Audio Signal Traces (EVB 1st Layer)

3.4.3. I2C Interface

Route I2C signal traces as a group and surround them with ground. The recommended space between I2C_SDA and I2C_SCL is 1.5 times of the trace width.

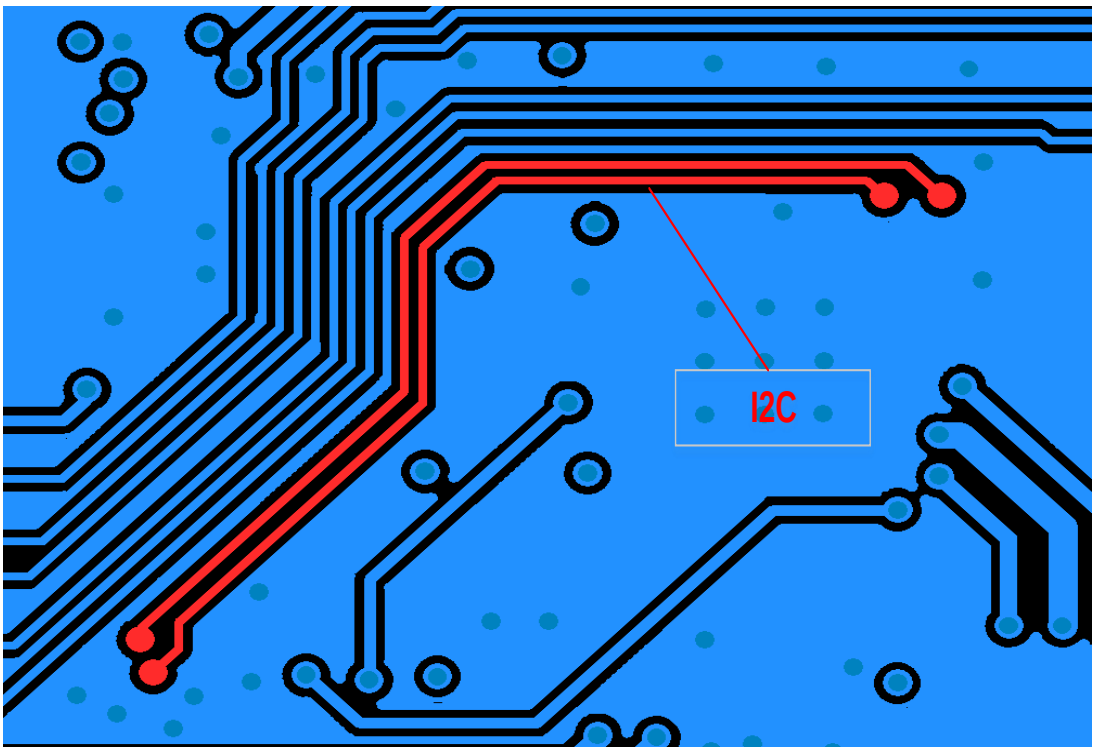

Figure 15: I2C Traces (ALC5616 TE-A 3rd Layer)

3.5. (U)SIM Interface

- Place the (U)SIM card connector near the module, and keep the trace length of (U)SIM card signals as short as possible. The total length of each (U)SIM signal trace should be less than 200 mm.
- It is suggested to route USIM_RST/CLK/DATA signal traces in the inner layer with total grounding and vias are kept near the pins. Keep them away from RF traces and VBAT power traces.
- If USIM_DATA and USIM_CLK traces cannot be routed with total grounding, separate them with USIM_RST and keep them away from each other and ensure that they are not routed in parallel.
- Filter capacitors and ESD protection component for USIM_VDD should be placed near the (U)SIM card connector.

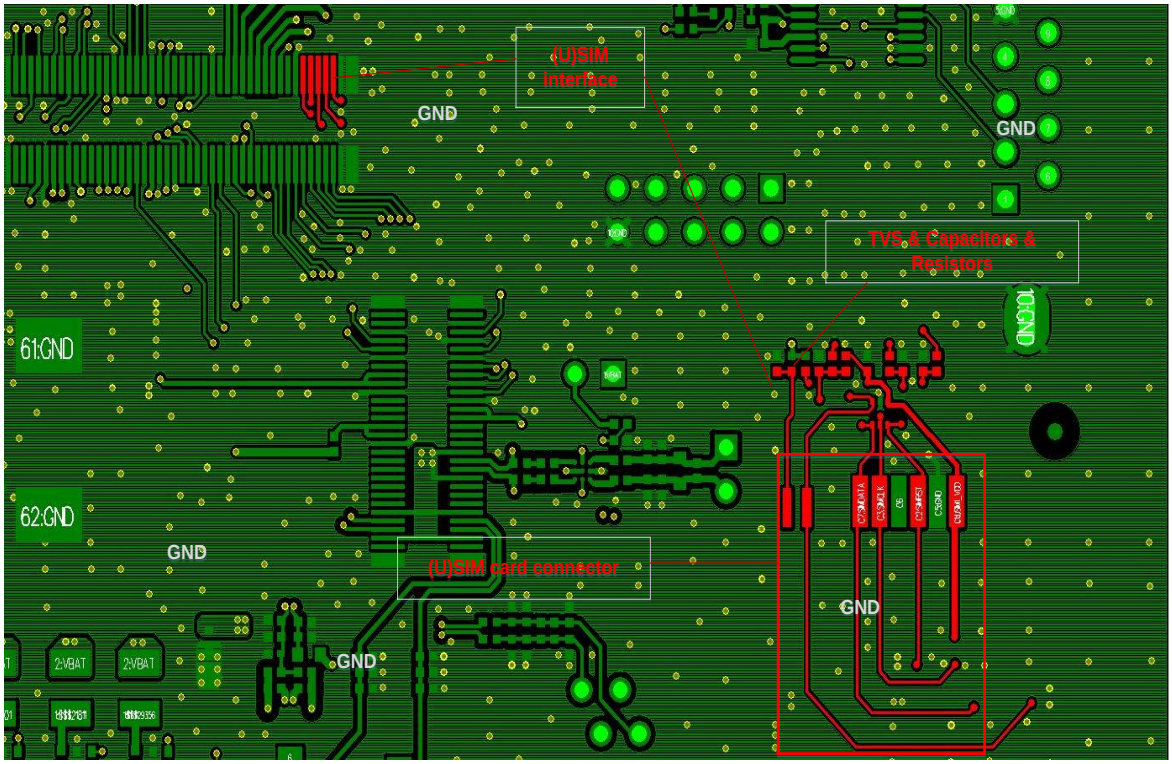

Figure 16: Overview of (U)SIM Signal Traces (EVB 1st Layer)

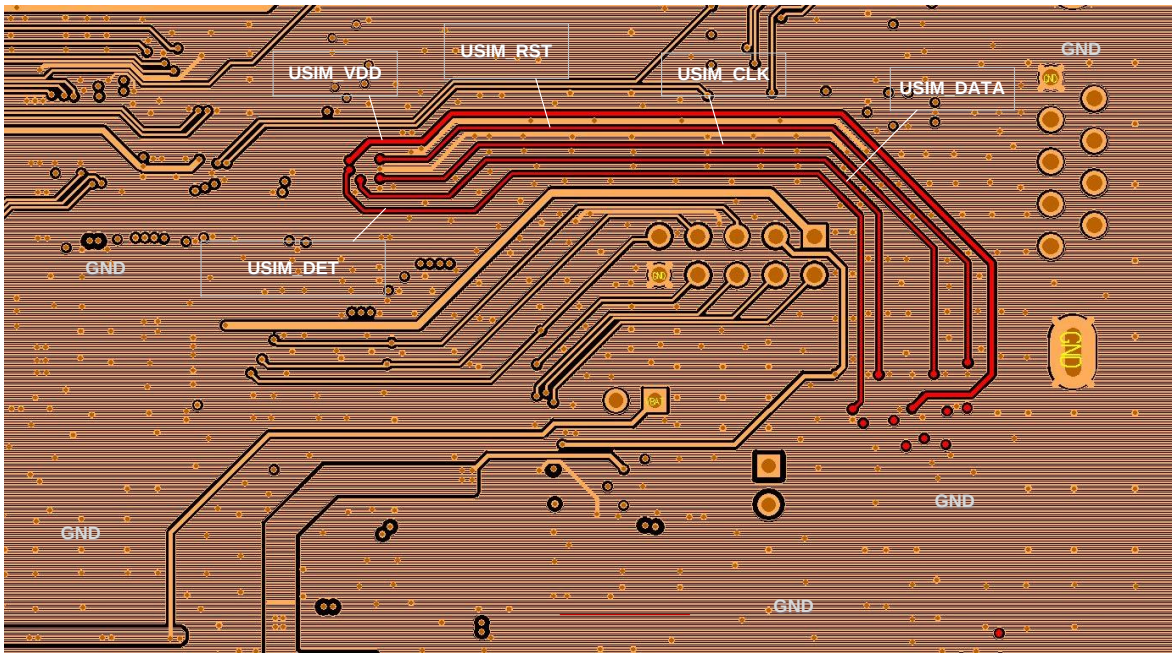

Figure 17: Overview of (U)SIM Signal Traces (EVB 2nd Layer)

3.6. ADC Interfaces

ADC belongs to analog signal and it is sensitive, so it is recommended to be ground surrounded and keep it away from interference sources.

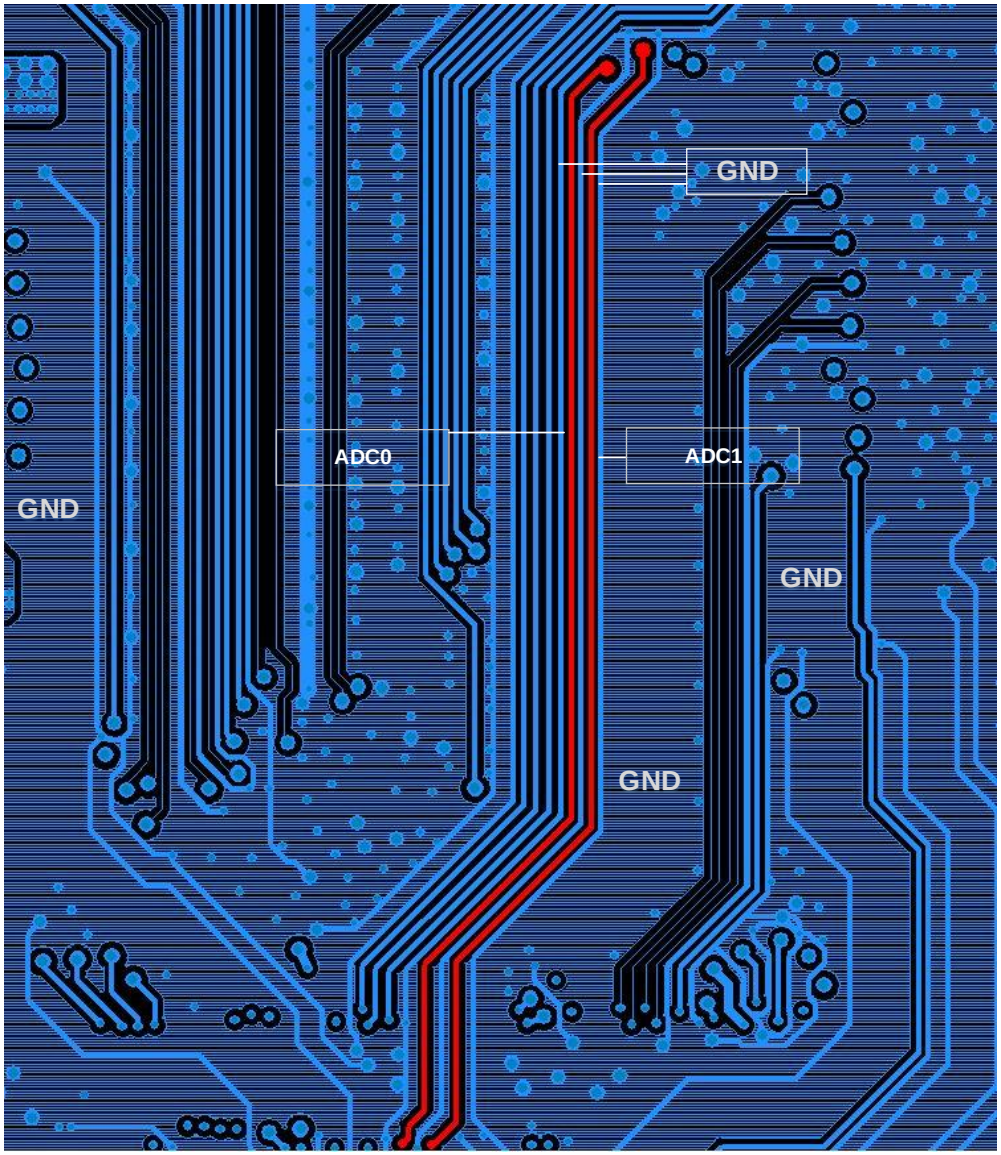

Figure 18: Overview of ADC Signal Traces (EVB 3rd Layer)

3.7. Antenna Interfaces

3.7.1. PCB Structures of Microstrip and Coplanar Waveguide

3.7.1.1. PCB Structure of Microstrip Waveguide

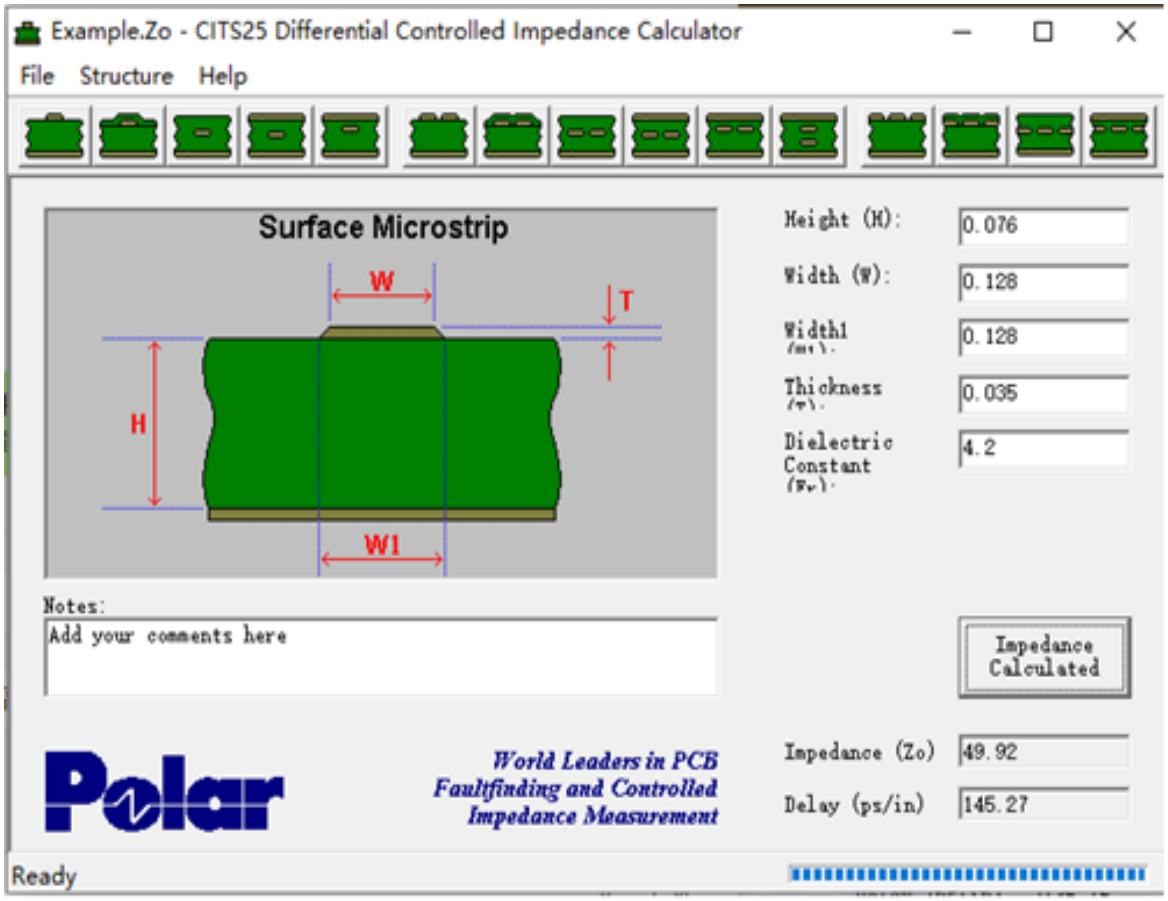

Figure 19: PCB Structure of Microstrip Waveguide

3.7.1.2. PCB Structure of Coplanar Waveguide

The factors which influence the impedance include dielectric constant (usually 4.2–4.6, 4.4 here), dielectric layer height (H), RF trace width (W), the space between RF trace and the ground (S), and copper thickness (T).

When T = 0.035 mm, the recommended values of W and S for 50 Ω coplanar waveguide under different PCB structures are listed in the table below.

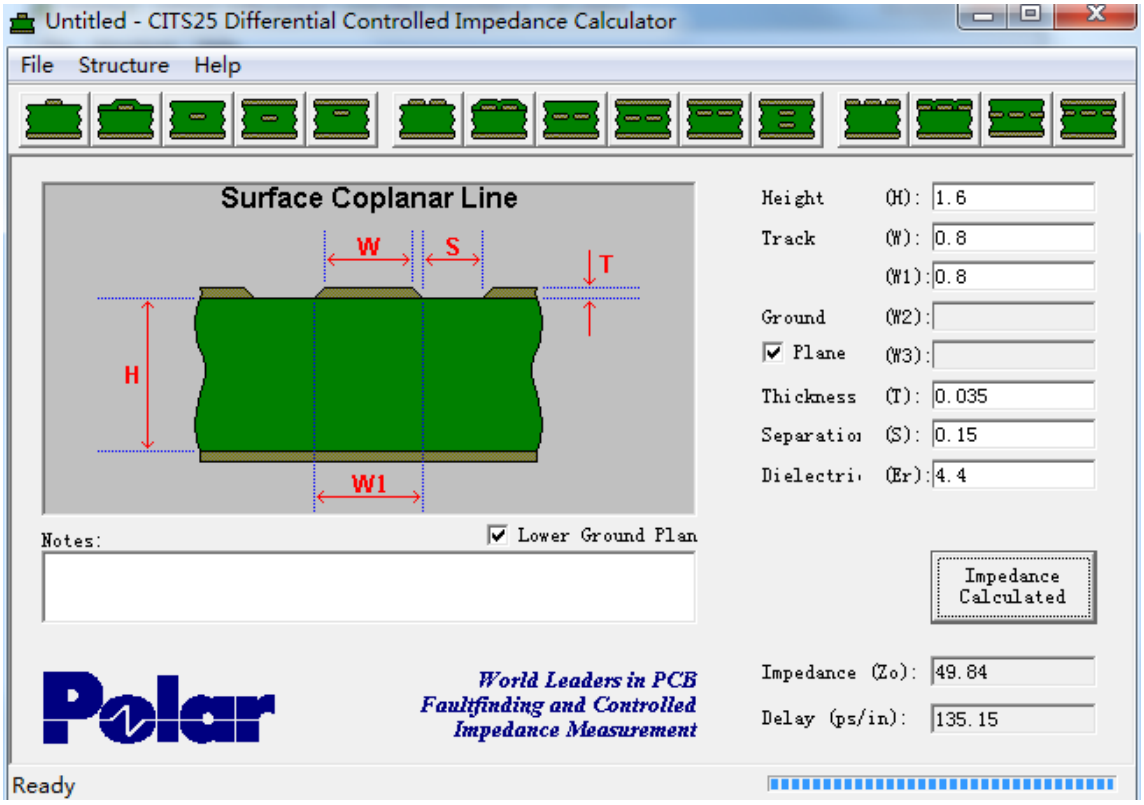

Figure 20: PCB Structure of Coplanar Waveguide

Table 1: Recommended Values of W and S (50 Ω Coplanar Waveguide under Different PCB Structures)

Dielectric Height (H)	RF Trace Width (W)	Space between RF Trace and the Ground (S)
0.076 mm	0.1188 mm	0.15 mm
0.1 mm	0.1623 mm	0.2 mm
0.15 mm	0.24 mm	0.2 mm
0.8 mm	0.8 mm	0.18 mm
1.0 mm	0.8 mm	0.17 mm
1.2 mm	0.8 mm	0.16 mm
1.6 mm	0.8 mm	0.15 mm
2 mm	0.8 mm	0.14 mm

3.7.2. Reference Design of RF Layout

If there is a 2-layer PCB, the top layer is for signal trace, and the bottom layer should be reference ground layer. If there is a 4-layer PCB, the reference ground layer could be the second layer, the third layer, or the fourth layer. If the third layer is chosen as the ground layer, the second layer should be kept out and the width of keep-out area should be at least 5 times of the trace width. See following figures for more details.

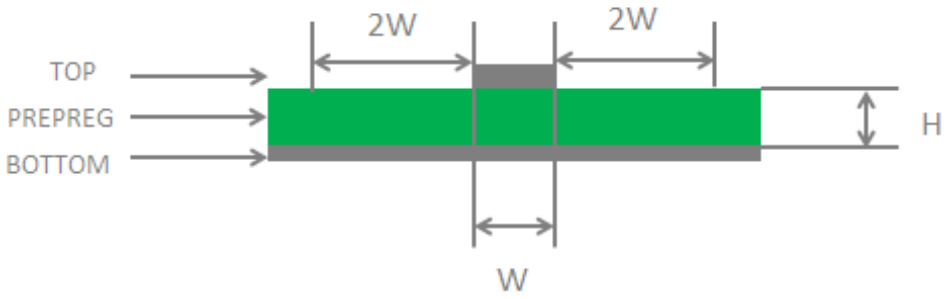

Figure 21: Microstrip Design on 2-layer PCB

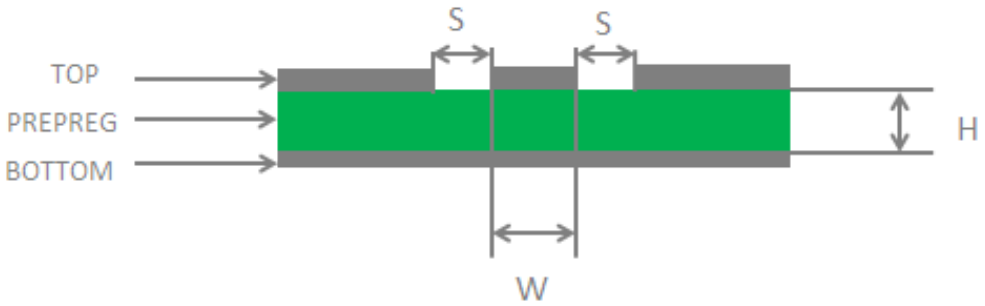

Figure 22: Coplanar Waveguide Design on 2-layer PCB

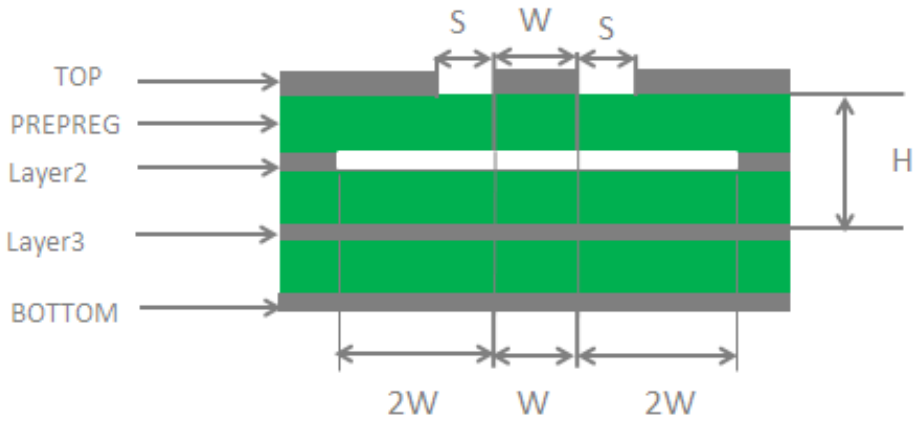

Figure 23: Coplanar Waveguide Design on 4-Layer PCB (3rd Layer as Reference Ground)

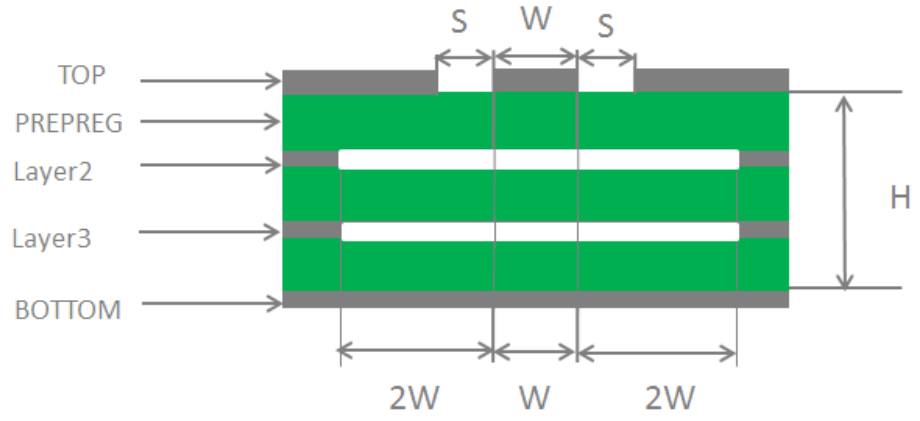

Figure 24: Coplanar Waveguide Design on 4-layer PCB (4th Layer as reference Ground)

3.7.3. Coplanar Waveguide PCB Layout

There are 6 guidelines should be taken into account, as marked in the figures below.

1. Keep the coplanar waveguide of 50 Ω corresponding to the suitable Width (W) and Space (S). Take FR4 (a common PCB material with dielectric constant of 4.2 to 4.6) and copper clad thickness of 35μm as an example, values of W and S for 50 Ω coplanar waveguide under different PCB structures are shown as ***Table 1***. The accuracy of W and S should be taken care of when manufacturing the PCB.

2. The GND pins next to the RF trace should be contacted with ground plane.

3. Leave a small keep-out area for the RF trace on the top layer to reduce parasitic effect. Keep the RF trace as short as possible. Avoid placing RF traces at 90 degrees, instead, a 135-degree placement is recommended.

4. Keep a certain distance between signal pads and ground when packaging the device. If the signal pad is SMD type, plate the copper on the corresponding signal pad.

5. Ensure that the reference ground plane corresponding to the RF trace is complete. Add as many ground vias as possible around the RF signal line to minimize EMI. The distance between GND vias and RF trace should be more than two times of trace width. Keep the ground plane for RF trace within the same layer and keep the ground plane as large as possible. Ensure that the reference ground plane in another layer is complete as well. Besides, the through vias for those two ground planes should be sufficient.

6. The pads for π-type matching circuit consisting of one resistor and two capacitors should be put near the module pin.

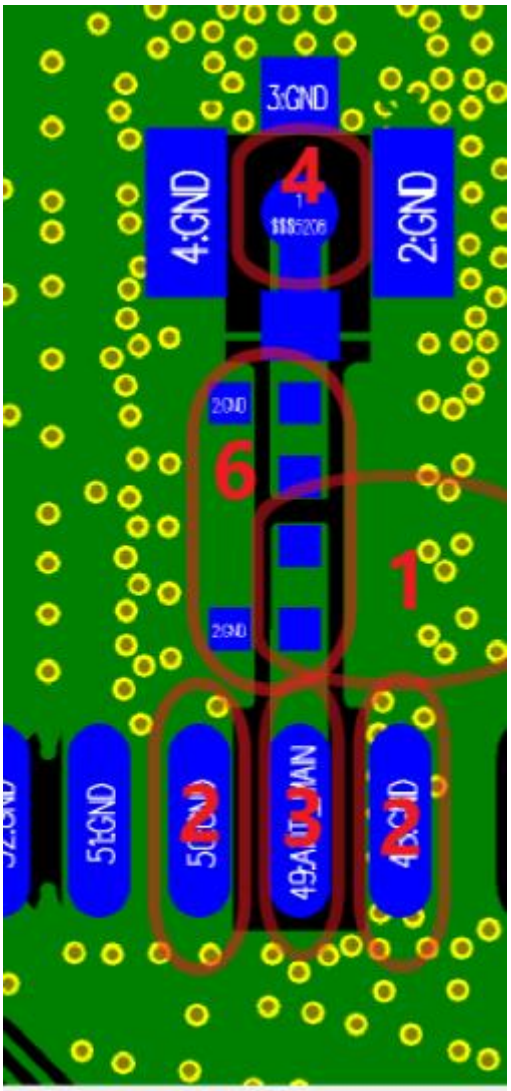

Figure 25: Overview of Antenna Signal Trace (TE-A 1st Layer)

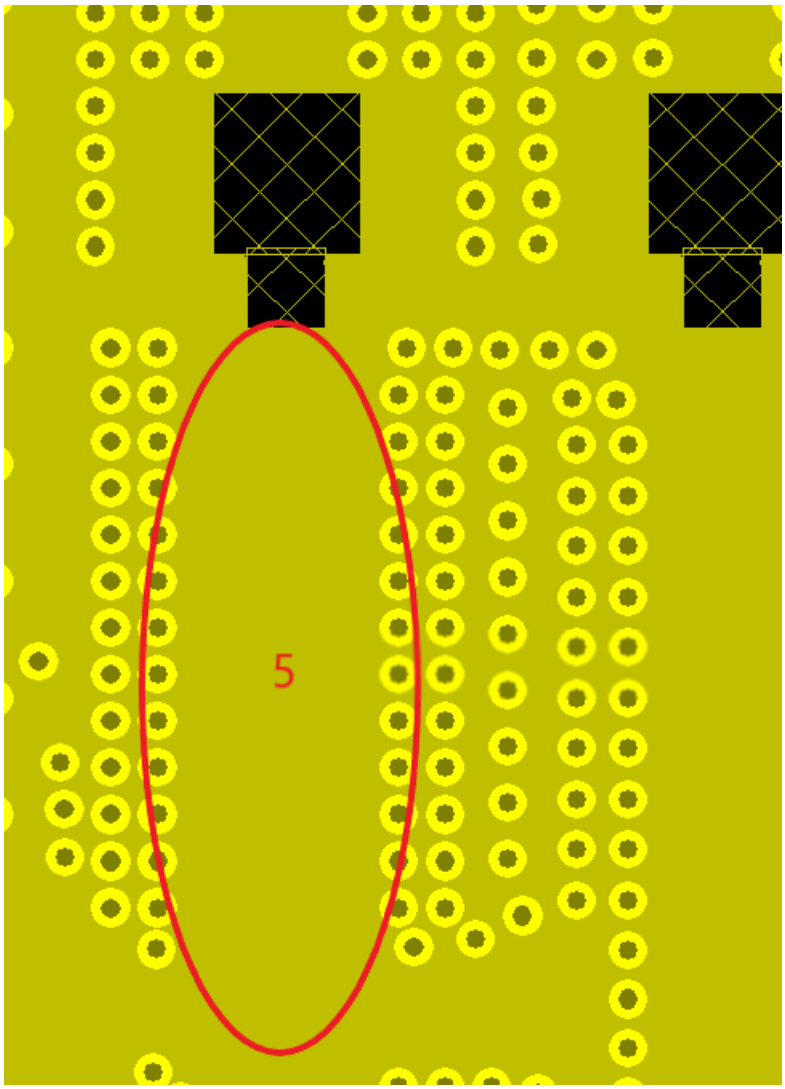

Figure 26: Overview of Antenna Signal Trace – Complete Reference Ground Plane (TE-A 2nd Layer)

4 Appendix References

Table 2: Related Documents

SN	Document Name	Remark
[1]	Quectel_BG95_Footprint&Part	BG95 series Footprint&Part
[2]	Quectel_BG96_Footprint&Part	BG96 Footprint&Part

Table 3: Terms and Abbreviations

Abbreviation	Description
ADC	Analog-to-Digital Converter
AGND	Analog Ground
CLK	Clock
CPU	Central Processing Unit
DGND	Digital Ground
DRAM	Dynamic Random-Access Memory
ESD	Electrostatic Discharge
EVB	Evaluation Board
FR	Flame Retardant
I2C	Inter-Integrated Circuit
IC	Integrated Circuit
LCD	Liquid Crystal Display
LPWA	Low-Power Wide-Area
LTE	Long-Term Evolution

PCB	Printed Circuit Board
PCM	Pulse Code Modulation
PMU	Power Management Unit
RC	Resister-Capacitor
RF	Radio Frequency
SMD	Surface Mount Device
SPI	Serial Peripheral Interface
TVS	Transient Voltage Suppressor
UART	Universal Asynchronous Receiver/Transmitter
UMTS	Universal Mobile Telecommunications System
USB	Universal Serial Bus
(U)SIM	(Universal) Subscriber Identity Module
VBAT	Voltage at Battery