FCM362K Hardware Design

Wi-Fi&Bluetooth Module Series

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Quectel Wireless Solutions Co., Ltd.
Building 5, Shanghai Business Park Phase III (Area B), No.1016 Tianlin Road, Minhang District, Shanghai 200233, China
Tel: +86 21 5108 6236
Email: info@quectel.com

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Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any terminal or mobile incorporating the module. Manufacturers of the terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for customers' failure to comply with these precautions.

	Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.
	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.
	Terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergency help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.
	The terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.
	In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other terminals. Areas with explosive or potentially explosive atmospheres include fueling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.

About the Document

Revision History

Version	Date	Author	Description
-	2023-11-17	Tara KONG/Vera SHI	Creation of the document
1.0.0	2023-11-17	Tara KONG/Vera SHI	Preliminary

Contents

Table Index

Figure Index

1 Introduction

QuecOpen® is a solution where the module acts as the main processor. Constant transition and evolution of both the communication technology and the market highlight its merits. It can help you to:

- Realize embedded applications' quick development and shorten product R&D cycle
- Simplify circuit and hardware structure design to reduce engineering costs
- Miniaturize products
- Reduce product power consumption
- Apply OTA technology
- Enhance product competitiveness and price-performance ratio

This document defines the FCM362K and describes its hardware interfaces and air interfaces which are connected with your applications. With this document, you can quickly understand module interface specifications, RF performances, electrical and mechanical details, as well as other related information of the module.

1.1. Special Marks

Table 1: Special Marks

Mark	Definition
*	Unless otherwise specified, when an asterisk (*) is used after a function, feature, interface, pin name, AT command, argument, and so on, it indicates that the function, feature, interface, pin, AT command, argument, and so on, is under development and currently not supported; and the asterisk (*) after a model indicates that the sample of the model is currently unavailable.
[…]	Brackets ([…]) used after a pin enclosing a range of numbers indicate all pins of the same type. For example, SDIO_DATA[0:3] refers to all four SDIO pins: SDIO_DATA0, SDIO_DATA1, SDIO_DATA2, and SDIO_DATA3.

2 Product Overview

FCM362K is a low-power and high-performance Wi-Fi 6 and Bluetooth 5.2 Combo module supporting IEEE 802.11a/b/g/n/ac/ax and Bluetooth 5.2 standard. The module provides multiple interfaces including SDIO, UART, SPI*, PCM*, I2C*, I2S*, PWM*, ADC*, and USB* for various applications.

It is an SMD module with compact packaging which includes:

- 240 MHz Cortex-M4F processor
- Built-in 896 KB ROM, 992 KB SRAM and 4 MB flash
- Support for secondary development

Table 2: Basic Information

FCM362K	
Packaging type	LCC
Pin counts	47
Dimensions	(25.5 ±0.2) mm × (18 ±0.2) mm × (3.15 ±0.2) mm
Weight	Approx. 1.41 g

2.1. Key Features

Table 3: Key Features

Basic Information	
Protocols and Standard	● Wi-Fi Protocols: IEEE 802.11a/b/g/n/ac/ax ● Bluetooth protocol: Bluetooth 5.2 ● All hardware components are fully compliant with EU RoHS directive
Power Supply	**VBAT Power Supply:** ● 3.0–3.6 V ● Typ.: 3.3 V
Temperature Ranges	● Operating temperature [1]: -40 to +85 °C ● Storage temperature: -45 to +95 °C
TE-B Kit	FCM362K-TE-B [2]
Antenna/Antenna Interface	
Antenna/Antenna Interfaces [3]	● Pin antenna interface (ANT_WIFI/BT) ● PCB antenna ● RF coaxial connector ● 50 Ω characteristic impedance
Application Interface [4]	
Application Interfaces	SDIO, UART, SPI*, PCM*, I2C*, I2S*, PWM*, ADC*, USB*

[1] Within the operating temperature range, the module's related performance meets IEEE and Bluetooth specifications.
[2] For more details about the TE-B, see ***document [1]***.
[3] The module is provided with one of the three antenna/antenna interface designs. For more details, please contact Quectel Technical Support.
[4] For more details about the interfaces, see ***Chapter 3.3*** and ***Chapter 3.4***.

2.2. Functional Diagram

The following figure shows a block diagram of the module and illustrates the major functional parts.

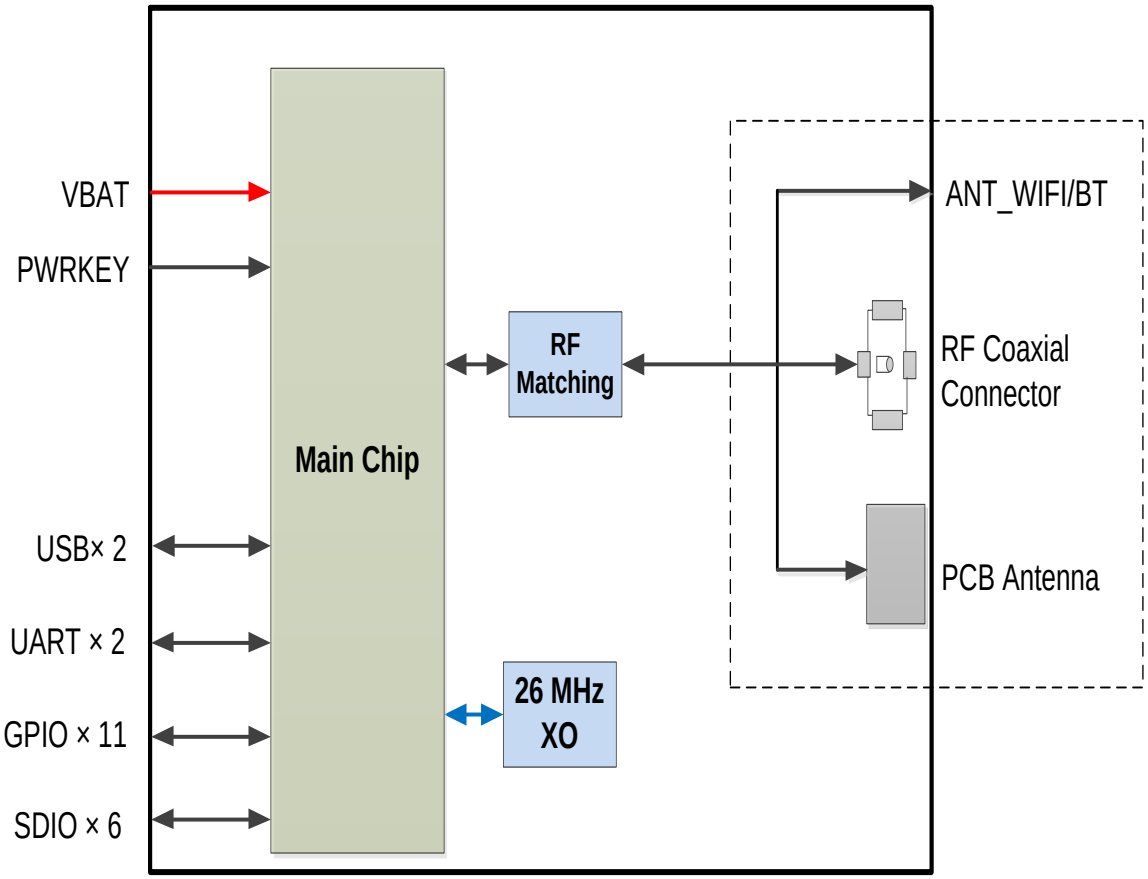


Figure 1: Functional Diagram

NOTE

1. The module is provided with one of the three antenna/antenna interface designs. For more details, please contact Quectel Technical Support.
2. The module has SDIO, UART, USB, and 11 GPIO interfaces by default. In the case of multiplexing, it supports interfaces including SPI*, PCM*, I2C*, I2S*, PWM*, and ADC*. For more details, see ***Chapter 3.3*** and ***Chapter 3.4***.

3 Application Interfaces

3.1. Pin Assignment

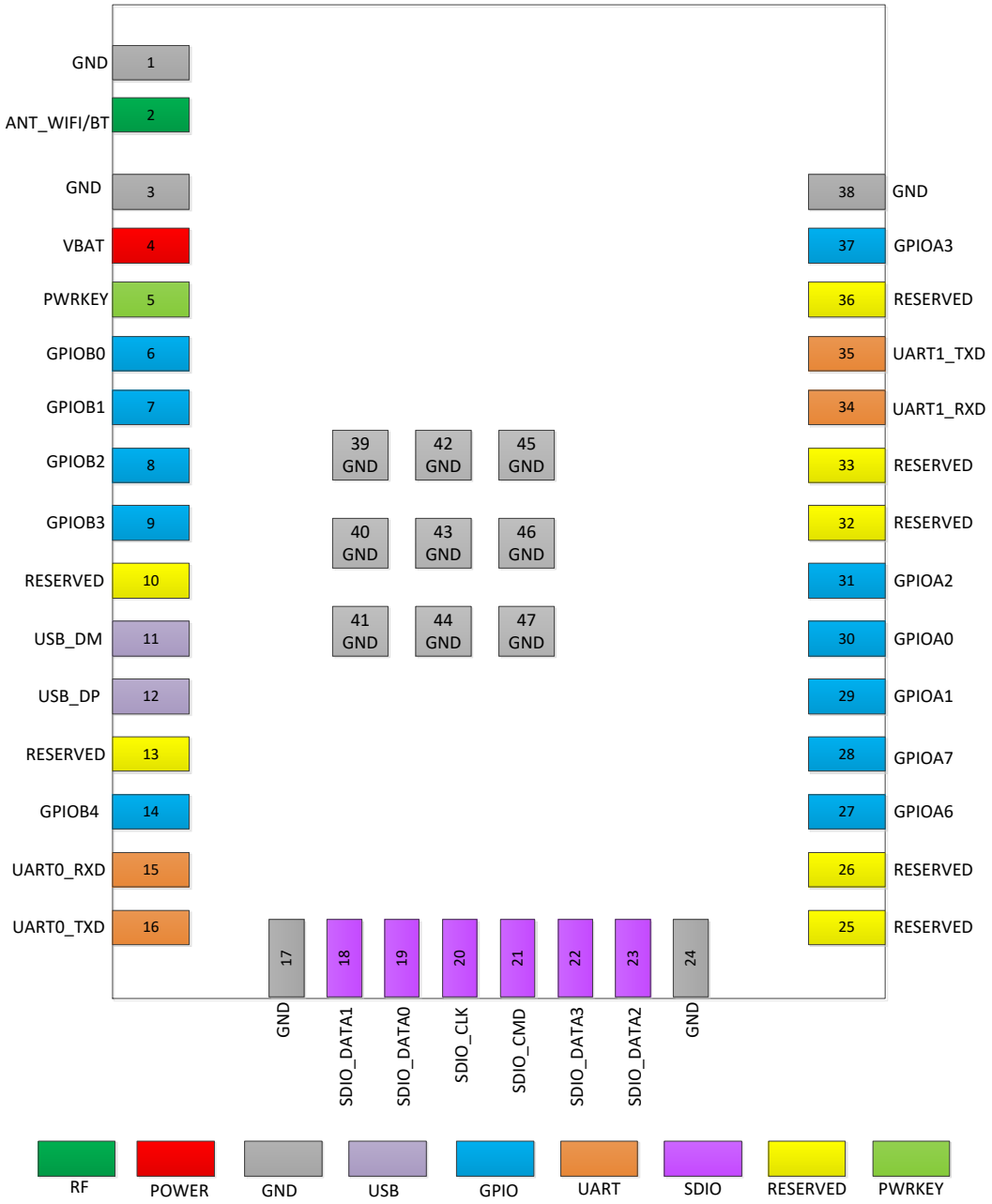


Figure 2: Pin Assignment (Top View)

NOTE

1. Keep all RESERVED and unused pins unconnected.
2. All GND pins should be connected to ground.
3. The module has SDIO, UART, USB, and 11 GPIO interfaces by default. In the case of multiplexing, it supports interfaces including SPI*, PCM*, I2C*, I2S*, PWM*, and ADC*. For more details, see ***Chapter 3.3*** and ***Chapter 3.4***.

3.2. Pin Description

Table 4: Parameter Definition

Parameter	Description
AIO	Analog Input/Output
DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output
PI	Power Input

DC characteristics include power domain and rated current.

Table 5: Pin Description

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT	4	PI	Power supply for the module	Vmax = 3.6 V Vmin = 3.0 V Vnom = 3.3 V	It must be provided with sufficient current of at least 0.5 A.
GND	1, 3, 17, 24, 38–47				
Turn on/off					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**

PWEKEY	5	DI	Turn on/off the module	VBAT	Internally pulled down with a 200 kΩ resistor. Active high.
UARTs					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
UART0_TXD	16	DO	UART0 transmit	VBAT	
UART0_RXD	15	DI	UART0 receive		
UART1_TXD	35	DO	UART1 transmit		
UART1_RXD	34	DI	UART1 receive		
USB Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_DP	12	AIO	USB 2.0 differential data (+)		Require differential impedance of 90 Ω. USB 2.0 compliant. Test points must be reserved.
USB_DM	11	AIO	USB 2.0 differential data (-)		
GPIO Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
GPIOA0	30	DIO	General-purpose input/output	VBAT	All GPIO supports wakeup.
GPIOA1	29	DIO	General-purpose input/output		
GPIOA2	31	DIO	General-purpose input/output		
GPIOA3	37	DIO	General-purpose input/output		
GPIOA6	27	DIO	General-purpose input/output		
GPIOA7	28	DIO	General-purpose input/output		
GPIOB0	6	DIO	General-purpose input/output		
GPIOB1	7	DIO	General-purpose input/output		

GPIOB2	8	DIO	General-purpose input/output		
GPIOB3	9	DIO	General-purpose input/output		
GPIOB4	14	DIO	General-purpose input/output		
SDIO Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SDIO_DATA0	19	DIO	SDIO data bit 0	VBAT	
SDIO_DATA1	18	DIO	SDIO data bit 1		
SDIO_DATA2	23	DIO	SDIO data bit 2		
SDIO_DATA3	22	DIO	SDIO data bit 3		
SDIO_CLK	20	DIO	SDIO clock		
SDIO_CMD	21	DIO	SDIO command		
RF Antenna Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ANT_WIFI/BT	2	AIO	Wi-Fi/Bluetooth antenna interface		50 Ω characteristic impedance.
RESERVED Pins					
Pin Name	**Pin No.**				**Comment**
RESERVED	10, 13, 25, 26, 32, 33, 36				Keep them open.

3.3. GPIO Multiplexing

The module has SDIO, UART, USB, and 11 GPIO interfaces by default, and can support up to 23 GPIO interfaces in the case of multiplexing. Pins are defined as follows:

Table 6: GPIO Multiplexing

Pin Name	Pin No.	Alternate Function 0 (GPIO No.)	Alternate Function 1	Alternate Function 2	Alternate Function 3	Alternate Function 4	Alternate Function 5	Alternate Function 6	Alternate Function 7	Alternate Function 8	Alternate Function 9
GPIOA0	30	GPIOA0	I2C1_SCL	I2S0_WS	PCM_SYNC	SPI_CLK	PWM0	PCM_DOUT	PCM_CLK	BT_CTS*	-
GPIOA1	29	GPIOA1	I2C1_SDA	I2S0_BCLK	PCM_CLK	SPI_CS0	PWM1	PCM_DIN	PCM_DOUT	BT_RTS*	-
GPIOA2	31	GPIOA2	URAT0_RXD	I2S0_DIN	PCM_DIN	SPI_MISO	PWM2	PCM_SYNC	PCM_DIN	BT_RXD*	UART1_RXD
GPIOA3	37	GPIOA3	UART0_TXD	I2S0_DOUT	PCM_DOUT	SPI_MOSI	-	PCM_CLK	PCM_SYNC	BT_TXD*	UART1_TXD
UART1_RXD	34	GPIOA4	UART0_CTS	I2S0_BCLK	PCM_SYNC	SPI_CD	-	-	-	BT_RXD*	UART1_CTS
UART1_TXD	35	GPIOA5	UART0_RTS	I2S0_WS	PCM_DIN	SPI_FMARK	-	-	-	BT_TXD*	UART1_RTS
GPIOA6	27	GPIOA6	I2C2_SCL	UART1_CTS	PCM_DOUT	SPI_CS1	-	-	UART2_RXD	BT_CTS*	BT_RXD*
GPIOA7	28	GPIOA7	I2C2_SDA	UART1_RTS	PCM_CLK	SPI_CS2	AON_PWM0	-	UART2_TXD	BT_RTS*	BT_TXD*
UART0_RXD	15	GPIOA8	-	-	-	-	-	-	UART2_CTS	-	BT_CTS*
UART0_TXD	16	GPIOA9	-	-	-	SPI_CS3	AON_PWM1	-	UART2_RTS	-	BT_RTS*
SDIO_DATA1	18	GPIOA10	UART1_RXD	I2S1_BCLK	UART2_RXD	SPI_CLK	BT_CTS	-	-	BT_CTS*	-
SDIO_DATA0	19	GPIOA11	UART1_TXD	I2S1_WS	UART2_TXD	SPI_CS0	BT_RTS	-	-	BT_RTS*	-
SDIO_CLK	20	GPIOA12	UART1_CTS	I2S1_DIN	UART2_CTS	SPI_MISO	AON_PWM2	-	PCM_SYNC	BT_RXD*	-
SDIO_CMD	21	GPIOA13	UART1_RTS	-	UART2_RTS	SPI_MOSI	PWM0	CODEC_MCLK	PCM_CLK	BT_TXD*	-
SDIO_DATA3	22	GPIOA14	I2C3_SCL	I2S1_DOUT	-	SPI_CD	PWM1	UART0_RXD	PCM_DIN	-	-
SDIO_DATA2	23	GPIOA15	I2C3_SDA	I2S0_DIN	-	SPI_FMARK	PWM2	UART0_TXD	PCM_DOUT	-	-
GPIOB0	6	GPIOB0	I2C4_SCL	SPI_CLK	-	-	AON_PWM0	PCM_SYNC	-	-	-
GPIOB1	7	GPIOB1	I2C4_SDA	SPI_CS0	-	-	AON_PWM1	PCM_CLK	-	-	-

GPIOB2	8	GPIOB2	-	SPI_MISO	ADC0	-	AON_PWM2	PCM_DIN	-	-	-
GPIOB3	9	GPIOB3	-	SPI_MOSI	ADC1	-	-	PCM_DOUT	-	-	-
GPIOB4	14	GPIOB4	PWM0	-	-	-	-	-	-	-	-
USB_DP	12	GPIOA20	-	-	-	-	-	-	-	-	-
USB_DM	11	GPIOA21	-	-	-	-	-	-	-	-	-

NOTE

1. All GPIO supports wakeup.
2. The maximum number of each application interface multiplexed with GPIOs is not available simultaneously. For more details, see ***Chapter 3.4***.

3.4. Interface Definition

3.4.1. SDIO Interfaces

The module provides an SDIO interface which complies with SDIO 3.0 specification. The interface supports both master and slave modes with maximum clock rate of up to 208 MHz and 1-bit (by default) and 4-bit data bus modes. It can read external SD card data in master mode and communicates with host in slave mode.

Table 7: Pin Definition of SDIO Interface

Pin Name	Pin No.	I/O	Description
SDIO_DATA0	19	DIO	SDIO data bit 0
SDIO_DATA1	18	DIO	SDIO data bit 1
SDIO_DATA2	23	DIO	SDIO data bit 2
SDIO_DATA3	22	DIO	SDIO data bit 3
SDIO_CLK	20	DIO	SDIO clock
SDIO_CMD	21	DIO	SDIO command

The following figure shows the SDIO connection in master and slave modes:

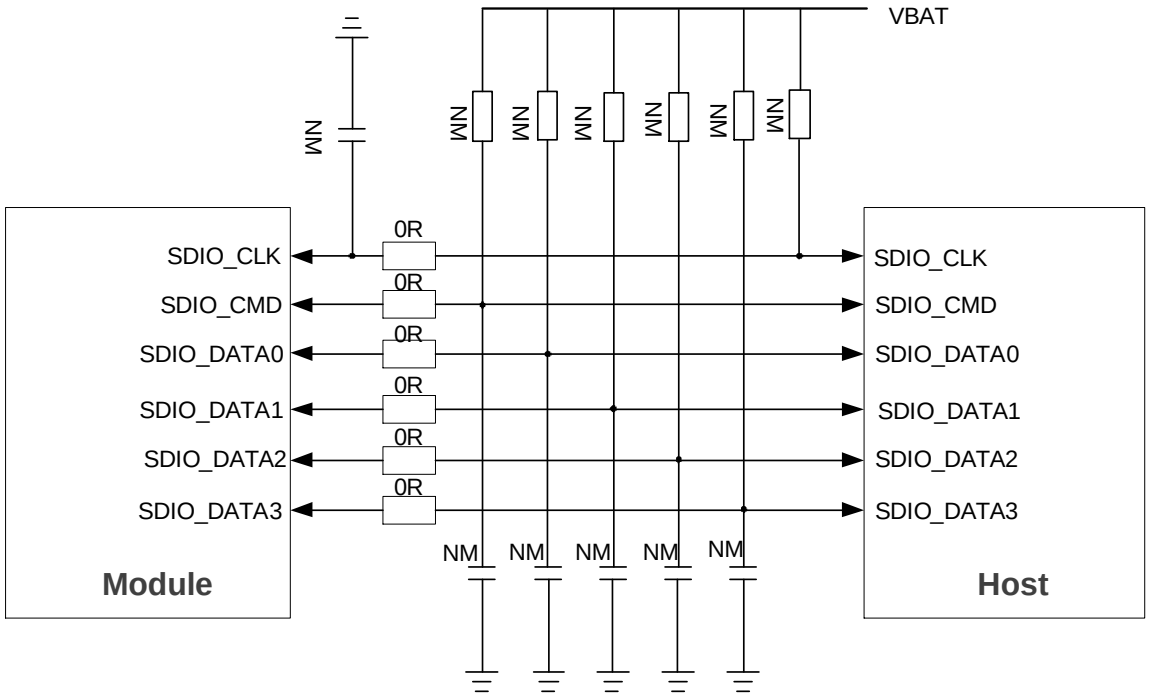


Figure 3: SDIO Connection

To ensure communication performance, the following conditions should be taken into considerations when designing SDIO interface:

- Route SDIO signal traces at the inner-layer of the PCB, and surround the traces with ground on that layer and with ground planes above and below. The impedance of SDIO signal trace is 70 Ω ±10 %.
- Keep SDIO signal traces far away from power supply traces, crystal-oscillators, magnetic devices, sensitive signals such as RF signals, analog signals, and noise signals generated by clock and DC-DC.
- SDIO_CLK, SDIO_DATA[0:3], and SDIO_CMD signal traces need to be of equal length (the distance between the traces should be less than 2.54 mm).
- Keep the adjacent trace clearance twice the trace width and the load capacitance of SDIO bus less than 15 pF.

3.4.2. UARTs

The module supports 2 UARTs (UART0 and UART1) by default. In the case of multiplexing, it can support up to 3 UARTS (UART0, UART1, and UART2).

Table 8: Pin Definition of UARTs

Pin Name	Pin No.	Alternate Function	I/O	Description	Comment
UART0_TXD	16	-	DO	UART0 transmit	Other UART configurations, see ***Table 6***.
UART0_RXD	15	-	DI	UART0 receive	
UART1_TXD	35	-	DO	UART1 transmit	
UART1_RXD	34	-	DI	UART1 receive	
GPIOA7	28	UART2_TXD	DO	UART2 transmit	
GPIOA6	27	UART2_RXD	DI	UART2receive	

UART1 and UART2 can be used for AT command communication and data transmission. The default baud rate is 115200 bps, and the maximum baud rate can reach 6 Mbps.

The main UART connection between the module and MCU is illustrated below.

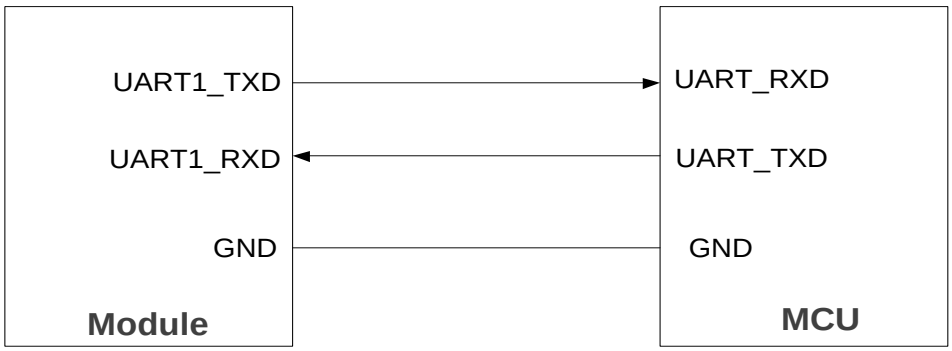


Figure 4: UART1 Connection

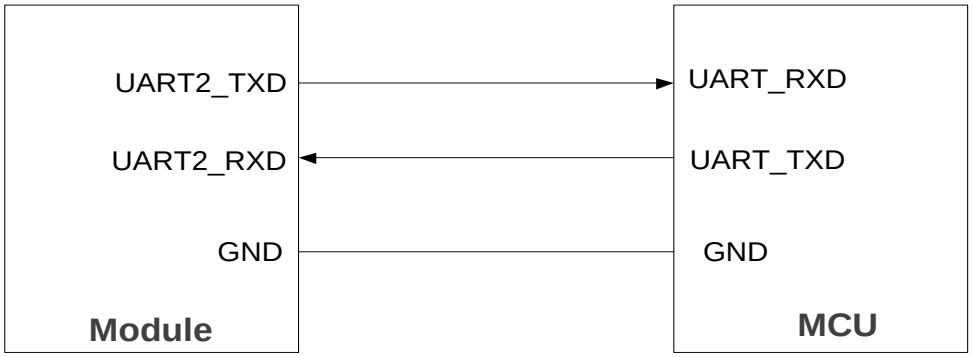


Figure 5: UART2 Connection

The debug UART0 supports 921600 bps baud rate by default, and is used for outputting partial logs with debugging tools. The following is a reference design of debug UART0. UART0 is also available for firmware upgrade and supports a configurable baud rate, with a default of 921600 bps.

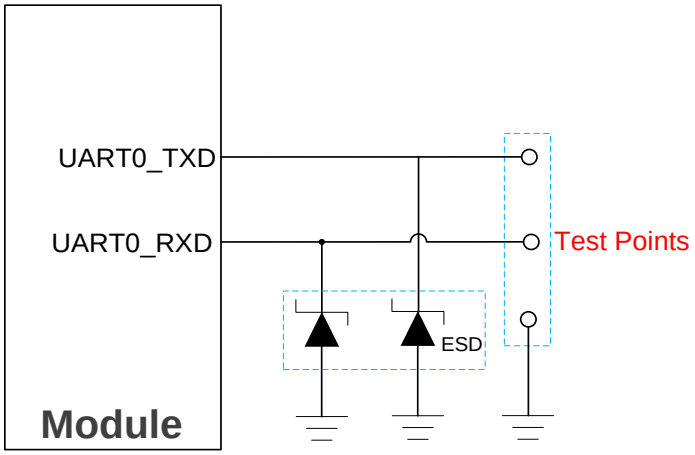


Figure 6: UART0 Reference Design

3.4.3. SPI*

In the case of multiplexing, the module provides 1 SPI which only supports master mode with a maximum clock frequency of up to 20 MHz.

Table 9: Pin Definition of SPI

Pin Name	Pin No.	Alternate Function	I/O	Description	Comment
GPIOA1	29	SPI_CS0	DO	SPI chip select	SPI supports 4 different addresses for chip select, and you can choose any one of them according to your needs.
GPIOA6	27	SPI_CS1	DO		
GPIOA7	28	SPI_CS2	DO		
UART0_TXD	16	SPI_CS3	DO		
GPIOA0	30	SPI_CLK	DO	SPI clock	Other SPI configurations, see ***Table 6***.
GPIOA2	31	SPI_MISO	DI	SPI master-in slave-out	
GPIOA3	37	SPI_MOSI	DO	SPI master-out slave-in	

The following figure shows the connection between the host and the slave:

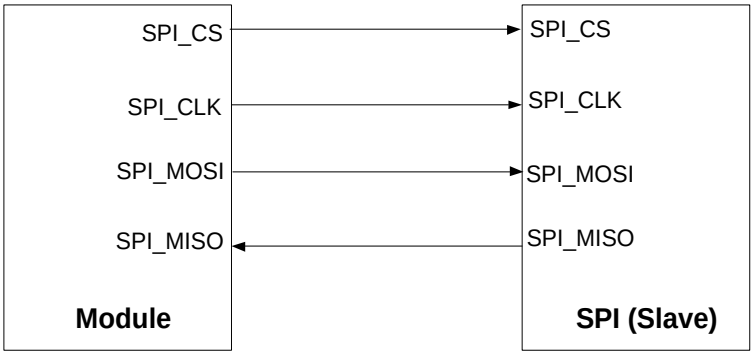


Figure 7: SPI Connection

3.4.4. PCM Interface*

In the case of multiplexing, the module supports 1 PCM channel.

Table 10: Pin Definition of PCM Interface

Pin Name	Pin No.	Alternate Function	I/O	Description	Comment
GPIOB0	6	PCM_SYNC	DIO	PCM data frame sync	Other PCM configurations, see ***Table 6***.
GPIOB1	7	PCM_CLK	DI	PCM clock	
GPIOB2	8	PCM_DIN	DI	PCM data input	
GPIOB3	9	PCM_DOUT	DO	PCM data output	
SDIO_CMD	21	CODEC_MCLK	DO	Clock output for codec	

3.4.5. I2C Interfaces*

In the case of multiplexing, the module provides up to 4 I2C interfaces that support master mode only. It supports:

- AMBA 2.0 APB bus protocol
- Standard-speed mode (100 kbps), high-speed mood (400 kbps) and fast-speed mode (3400 kbps) protocols
- Programmable master mode
- 7-bit and 10-bit addressing modes
- Programmable clock and data timing

- DMA
- Universal call address

Table 11: Pin Definition of I2C Interfaces

Pin Name	Pin No.	Alternate Function	I/O	Description
GPIOA0	30	I2C1_SCL	OD	I2C1 serial clock
GPIOA1	29	I2C1_SDA	OD	I2C1 serial data
GPIOA6	27	I2C2_SCL	OD	I2C2 serial clock
GPIOA7	28	I2C2_SDA	OD	I2C2 serial data
SDIO_DATA3	22	I2C3_SCL	OD	I2C3 serial clock
SDIO_DATA2	23	I2C3_SDA	OD	I2C3 serial data
GPIOB0	6	I2C4_SCL	OD	I2C4 serial clock
GPIOB1	7	I2C4_SDA	OD	I2C4 serial data

3.4.6. I2S Interface*

In the case of multiplexing, the module provides two I2S interface which supports both master and slave modes with sampling rates from 8 kHz to 384 kHz.

Table 12: Pin Definition of I2S Interface

Pin Name	Pin No.	Alternate Function	I/O	Description	Comment
GPIOA0	30	I2S0_WS	DO	I2S0 channel select	Other I2S configurations, see ***Table 6***.
GPIOA1	29	I2S0_BCLK	DO	I2S0 bit clock	
GPIOA2	31	I2S0_DIN	DI	I2S0 data input	
GPIOA3	37	I2S0_DOUT	DO	I2S0 data output	
SDIO_DATA0	19	I2S1_WS	DO	I2S0 bit clock	
SDIO_DATA1	18	I2S1_BCLK	DO	I2S0 channel select	
SDIO_CLK	20	I2S1_DIN	DI	I2S0 data input	

SDIO_DATA3	22	I2S1_DOUT	DO	I2S0 data output

3.4.7. PWM Interfaces*

In the case of multiplexing, the module supports up to 6 PWM channels.

Table 13: Pin Definition of PWM Interfaces

Pin Name	Pin No.	Alternate Function	I/O	Description	Comment
GPIOA0	30	PWM0	DO	PWM out	Other PWM configurations, see ***Table 6***.
GPIOA1	29	PWM1	DO	PWM out	
GPIOA2	31	PWM2	DO	PWM out	
GPIOA7	28	AON_PWM0	DO	PWM out (available in low power mode)	
UART0_TXD	16	AON_PWM1	DO	PWM out (available in low power mode)	
SDIO_CLK	20	AON_PWM2	DO	PWM out (available in low power mode)	

3.4.8. ADC Interfaces*

In the case of multiplexing, the module supports two 14-bit ADC interfaces, whose voltage range is 0–1.2 V. To improve ADC accuracy, surround ADC trace with ground.

Table 14: Pin Definition of ADC Interfaces

Pin Name	Pin No.	Alternate Function	I/O	Description
GPIOB2	8	ADC0	AI	General-purpose ADC interface
GPIOB3	9	ADC1	AI	General-purpose ADC interface

Table 15: ADC Features

Parameter	Min.	Typ.	Max.	Unit
ADC Voltage Range	0	-	1.2	V

ADC Resolution Rate	-	TBD	-	bit

3.4.9. USB Interface*

The module provides 1 integrated Universal Serial Bus (USB) interface as device which complies with the USB 2.0 specification and supports high-speed (480 Mbps) mode and is backward-compatible with full-speed (12 Mbps) mode.

Table 16: Pin Definition of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_DP	12	AIO	USB 2.0 differential data (+)	Require differential impedance of 90 Ω. USB 2.0 compliant. Test points must be reserved.
USB_DM	11	AIO	USB 2.0 differential data (-)	

The following figure shows the USB interface connection between the module and the host.

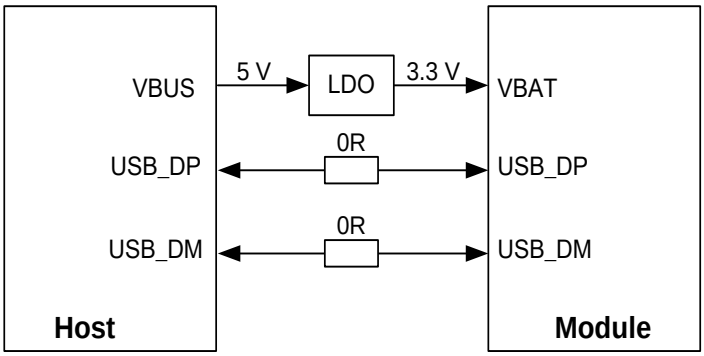


Figure 8: USB Interface Connection

When designing the USB interface, you should follow the following principles to meet USB 2.0 specifications.

- Route the USB signal traces as differential pairs with ground on the same layer and with ground planes above and below. The differential impedance of USB 2.0 is 90 Ω ±10 %.
- Do not route signal traces under crystals, oscillators, magnetic devices, sensitive circuits/signals, such as RF circuits and analog signals, as well as noisy signals such as clock signals and DC-DC signals.
- Reserve a 0 Ω resistor on USB_DP and USB_DM lines respectively if possible.

For more details about the USB 2.0 specifications, visit http://www.usb.org/home.

4 Operating Characteristics

4.1. Power Supply

Table 17: Pin Definition of Power Supply and GND Pins

Pin Name	Pin No.	I/O	Description	Min.	Typ.	Max.	Unit
VBAT	4	PI	Power supply for the module	3.0	3.3	3.6	V
GND	1, 3, 17, 24, 38–47						

4.1.1. Reference Design for Power Supply

The module is powered by VBAT, and it is recommended to use a power supply chip that can provide with sufficient current of at least 0.5 A. For better power supply performance, it is recommended to parallel a 22 μF decoupling capacitor, and two filter capacitors (1 μF and 100 nF) near the module's VBAT pin. And C4 is reserved for debugging and not mounted by default. In addition, it is recommended to add a TVS near the VBAT to improve the surge voltage bearing capacity of the module. In principle, the longer the VBAT trace is, the wider it should be.

VBAT reference circuit is shown below:

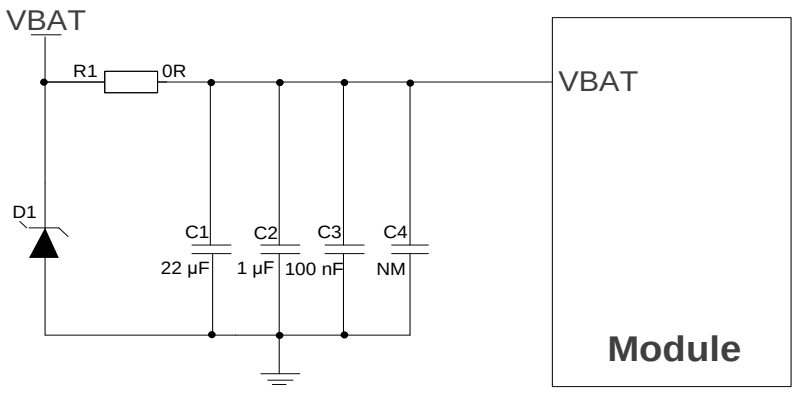


Figure 9: Reference Design of Power Supply

4.2. Turn On

After the VBAT is powered up, pull the PWRKEY up for 6 ms when turn on the module for the first time. When the module is completely powered off, the PWEKEY must be pulled up for 6 ms to start the module again.

Table 18: Pin Definition of PWRKEY

Pin Name	Pin No.	I/O	Description	Comment
PWRKEY	5	DI	Turn on/off the module	Internally pulled down with a 200 kΩ resistor. Active high.

The turn-on timing is shown below:

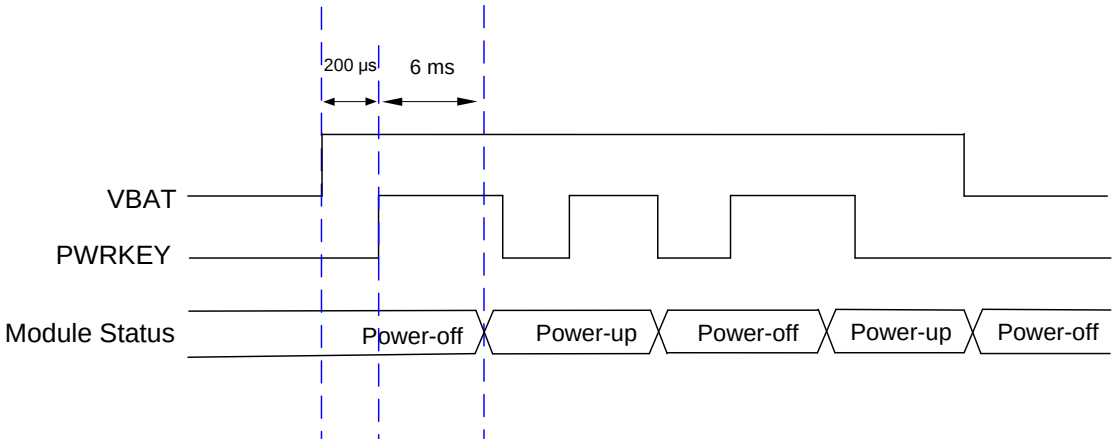


Figure 10: Turn-on Timing

4.3. Download Mode

After the module is powered up, keep the input of GPIOB0 and GPIOB1 at low level and press PWRKEY to start the module, and the module will enter the download mode. Firmware can be downloaded through UART0 in download mode.

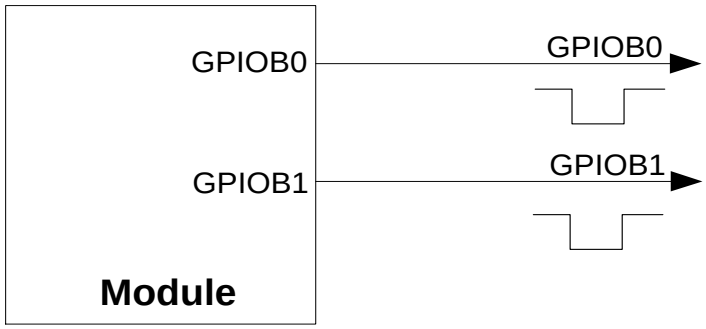


Figure 11: Reference Design for Download Mode

5 RF Performances

5.1. Wi-Fi Performances

Table 19: Wi-Fi Performances

Operating Frequency				
● **2.4 GHz:** 2.400–2.4835 GHz ● **5 GHz:** 5.150~5.850 GHz				
Modulation				
BPSK, QPSK, CCK, 16QAM, 64QAM, 256QAM, 1024QAM				
Encryption Mode				
WEP/WPA-PSK/WPA2/WPA3-SAE, MFP				
Operating Mode				
● AP ● STA				
Transmission Data Rate				
● 802.11b: 1 Mbps, 2 Mbps, 5.5 Mbps, 11 Mbps ● 802.11a/g: 6 Mbps, 9 Mbps, 12 Mbps, 18 Mbps, 24 Mbps, 36 Mbps, 48 Mbps, 54 Mbps ● 802.11n: HT20 (MCS 0–7), HT40 (MCS 0–7) ● 802.11ac: VHT20 (MCS 0–8), VHT40 (MCS 0–9) ● 802.11ax: HE20 (MCS 0–11), HE40 (MCS 0–11)				
Condition (VBAT = 3.3 V, Temp.: 25 ℃)		**EVM**	**Typ.; Unit: dBm; Tolerance: ±2 dB**	
			Transmitting Power	**Receiving Sensitivity**
2.4 GHz	802.11b @ 1 Mbps	≤ 35 %	18	-99
	802.11b @ 11 Mbps		18	-90
	802.11g @ 6 Mbps	≤ -5 dB	18	-93.5

	802.11g @ 54 Mbps	≤ -25 dB	15	-78
	802.11n, HT20 @ MCS 0	≤ -5 dB	18	-95
	802.11n, HT20 @ MCS 7	≤ -27 dB	15	-76.5
	802.11n, HT40 @ MCS 0	≤ -5 dB	18	-91.5
	802.11n, HT40 @ MCS 7	≤ -27 dB	15	-73
	802.11ax, HE20 @ MCS 0	≤ -5 dB	18	-94
	802.11ax, HE20 @ MCS 11	≤ -35 dB	13	-67
	802.11ax, HE40 @ MCS 0	≤ -5 dB	18	-92
	802.11ax, HE40 @ MCS 11	≤ -35 dB	13	-63
5 GHz	802.11a @ 6 Mbps	≤ -5 dB	18	-94.5
	802.11a @ 54 Mbps	≤ -25 dB	15	-78.5
	802.11n, HT20 @ MCS 0	≤ -5 dB	18	-94.5
	802.11n, HT20 @ MCS 7	≤ -27 dB	15	-76.5
	802.11n, HT40 @ MCS 0	≤ -5 dB	18	-91.5
	802.11n, HT40 @ MCS 7	≤ -27 dB	15	-73
	802.11ac, VHT20 @ MCS 0	≤ -5 dB	18	-95
	802.11ac, VHT20 @ MCS 8	≤ -27 dB	14	-72
	802.11ac, VHT40 @ MCS 0	≤ -5 dB	18	-91.5
	802.11ac, VHT40 @ MCS 9	≤ -32 dB	14	-67
	802.11ax, HE20 @ MCS 0	≤ -5 dB	18	-95
	802.11ax, HE20 @ MCS 11	≤ -32 dB	12	-67
	802.11ax, HE40 @ MCS 0	≤ -5 dB	18	-94.5
	802.11ax, HE40 @ MCS 11	≤ -30 dB	12	-63

5.2. Bluetooth Performances

Table 20: Bluetooth Performances

Operating Frequency		
2.400~2.4835 GHz		
Modulation		
GFSK, π/4-DQPSK, 8-DPSK		
Operating Mode		
● Classic Bluetooth (BR + EDR) ● Bluetooth Low Energy (BLE)		
Condition (VBAT = 3.3 V; Temp.: 25 ℃)	**Unit: dBm; Tolerance: ±3 dB**	
	Transmitting Power	**Receiving Sensitivity**
BR	3.59	-90
EDR (π/4-DQPSK)	0.14	-91
EDR (8-DPSK)	0.10	-85.5
BLE	3.55	-90

5.3. Antenna/ Antenna Interfaces [5]

The module is provided with one of the three antenna/antenna interface designs: pin antenna interface (ANT_WIFI/BT), PCB antenna and RF coaxial connector. The RF coaxial connector is not soldered when the module is designed with a PCB antenna or ANT_WIFI/BT antenna interface. The impedance of antenna port is 50 Ω.

Appropriate antenna type and design should be used with matched antenna parameters according to specific application. It is required to perform a comprehensive functional test for the RF design before mass production of terminal products. The entire content of this chapter is provided for illustration only. Analysis, evaluation and determination are still necessary when designing target products.

[5] The module is provided with one of the three antenna/antenna interface designs. For more details, please contact Quectel Technical Support.

5.3.1. Pin Antenna Interface (ANT_WIFI/BT)

Table 21: ANT_WIFI/BT Pin Definition

Pin Name	Pin No.	I/O	Description	Comment
ANT_WIFI/BT	2	AIO	Wi-Fi/Bluetooth antenna interface	50 Ω characteristic impedance.

5.3.1.1. Reference Design

For better RF performance, it is necessary to reserve a π-type matching circuit and add an ESD protection component. Matching components such as R1, C1, C2, and D1 should be placed as close to the antenna as possible. C1, C2, and D1 are not mounted by default. The parasitic capacitance of TVS should be less than 0.05 pF and R1 is recommended to be 0 Ω.

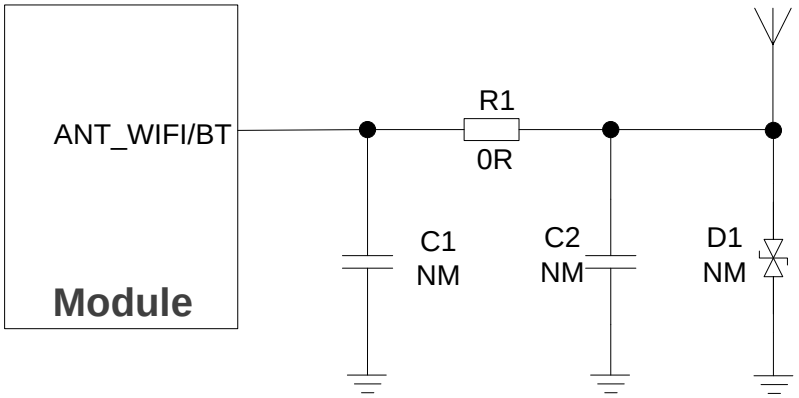


Figure 12: RF Antenna Reference Design

5.3.1.2. Antenna Design Requirements

Table 22: Antenna Design Requirements

Parameter	Requirement
Frequency Range (GHz)	2.4 GHz: 2.400–2.4835 5 GHz: 5.150–5.850
Cable Insertion Loss (dB)	< 1
VSWR	≤ 2 (Typ.)

Gain (dBi)	1 (Typ.)
Max. input power (W)	50
Input impedance (Ω)	50
Polarization type	Vertical

5.3.1.3. RF Routing Guidelines

For user's PCB, the characteristic impedance of all RF traces should be controlled to 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the height from the reference ground to the signal layer (H), and the spacing between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

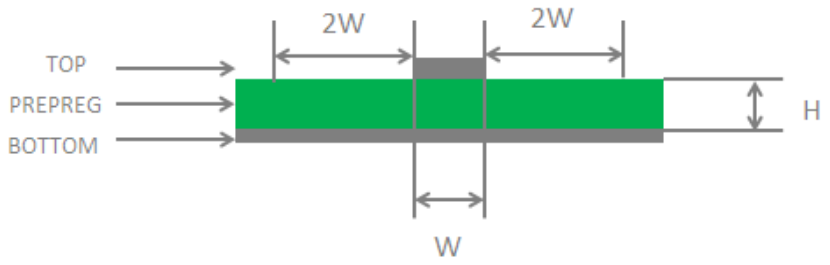


Figure 13: Microstrip Design on a 2-layer PCB

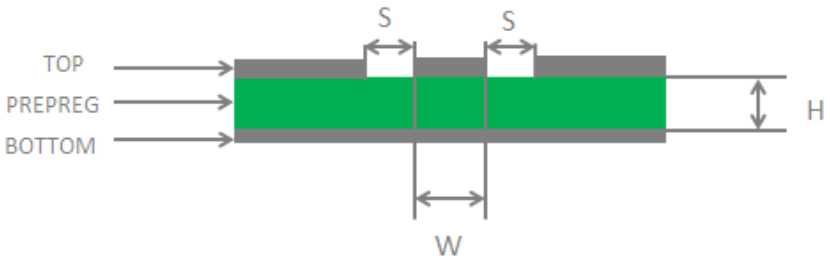


Figure 14: Coplanar Waveguide Design on a 2-layer PCB

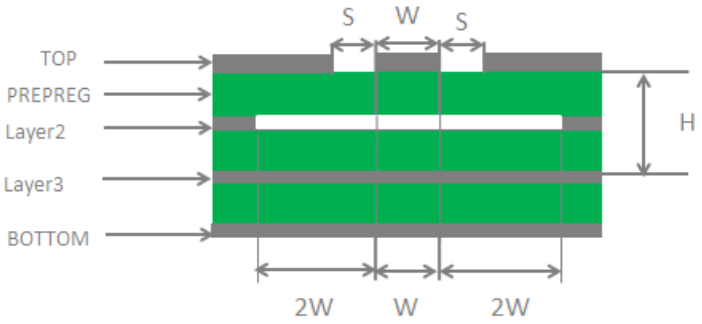


Figure 15: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

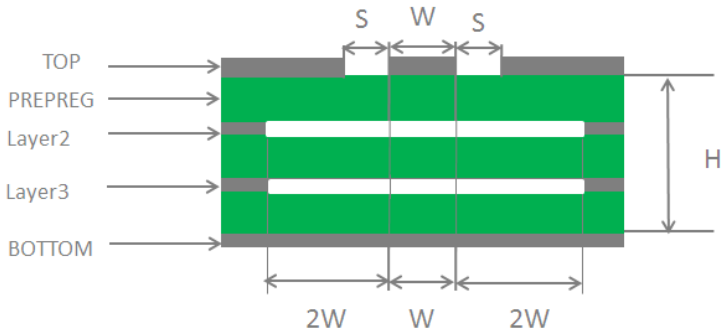


Figure 16: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

To ensure RF performance and reliability, follow the principles below in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible and all the right-angle traces should be changed to curved ones. The recommended trace angle is 135°.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be not less than twice the width of RF signal traces (2 × W).
- Keep RF traces away from interference sources, and avoid intersection and paralleling between traces on adjacent layers.

For more details about RF layout, see ***document [2]***.

5.3.1.4. RF Connector Recommendation

If RF connector is used for antenna connection, it is recommended to use the U.FL-R-SMT connector provided by Hirose.

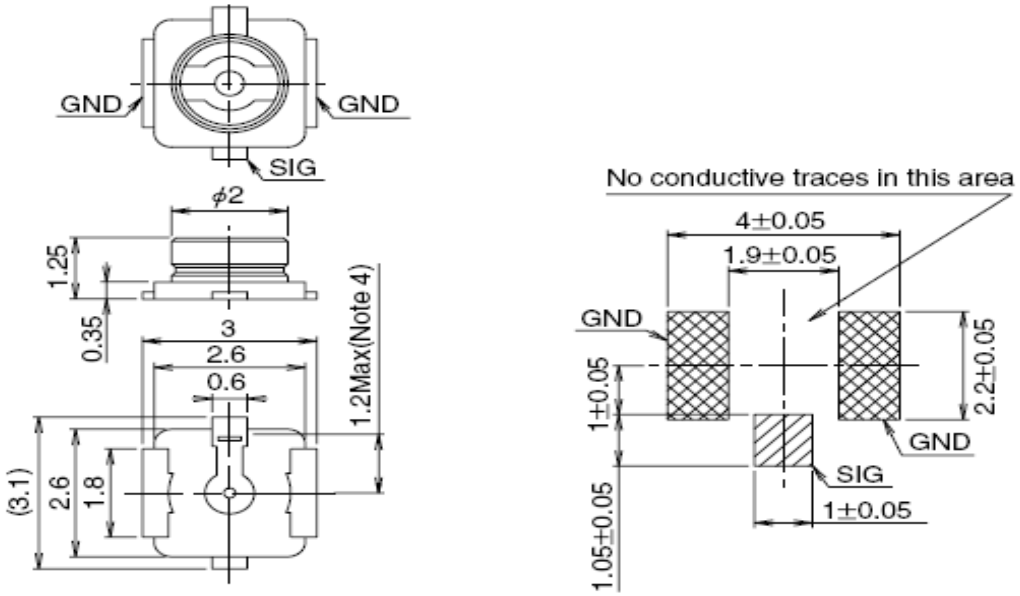


Figure 17: Dimensions of the Receptacle (Unit: mm)

U.FL-LP series mated plugs listed in the following figure can be used to match the U.FL-R-SMT connector.

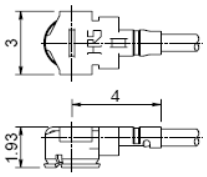
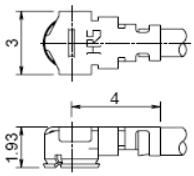
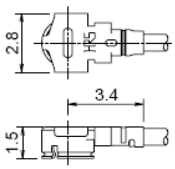
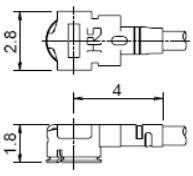
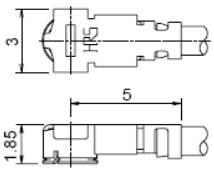
Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 18: Specifications of Mated Plugs

The following figure describes the space factor of mated connectors.

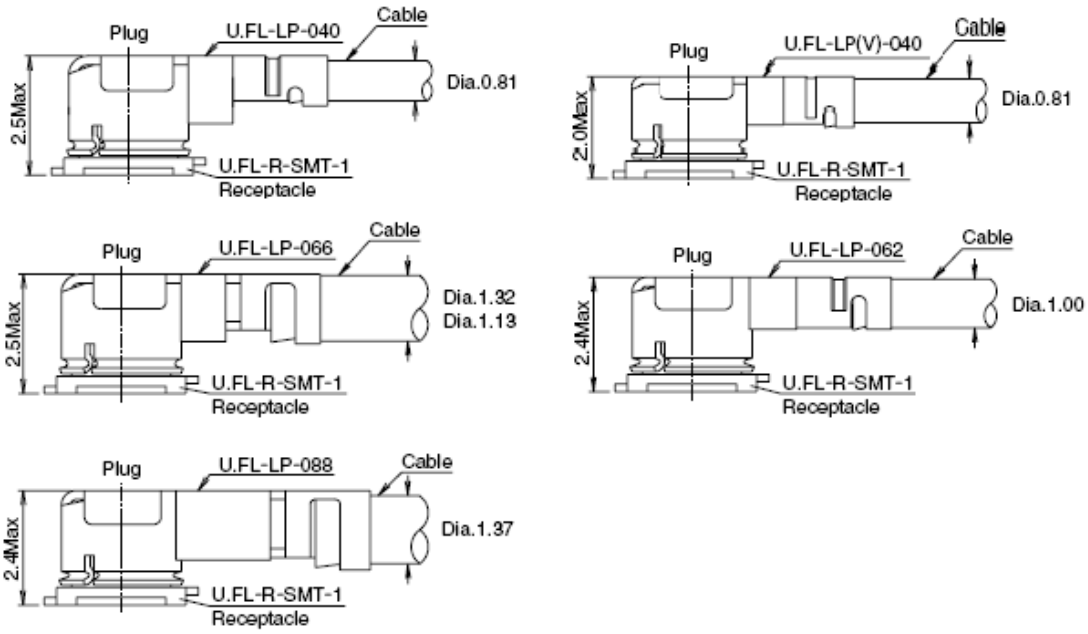


Figure 19: Space Factor of Mated Connectors (Unit: mm)

For more details, please visit http://www.hirose.com.

5.3.2. PCB Antenna

Table 23: PCB Antenna Specifications

Parameter	Requirement
Frequency Range (GHz)	2.4 GHz: 2.400–2.500 5GHz：5.150~5.850
Input Impedance (Ω)	50
VSWR	≤ 4
Gain (dBi)	-0.38 (Typ.)
Efficiency	30 %

When designed with PCB antenna, the module should be placed on the edge of the motherboard. The PCB antenna should be at least 16 mm away from the metal components, connectors, vias, traces, and copper pour area on the motherboard. All layers in the PCB of the motherboard under the PCB antenna should be designed as a keepout area.

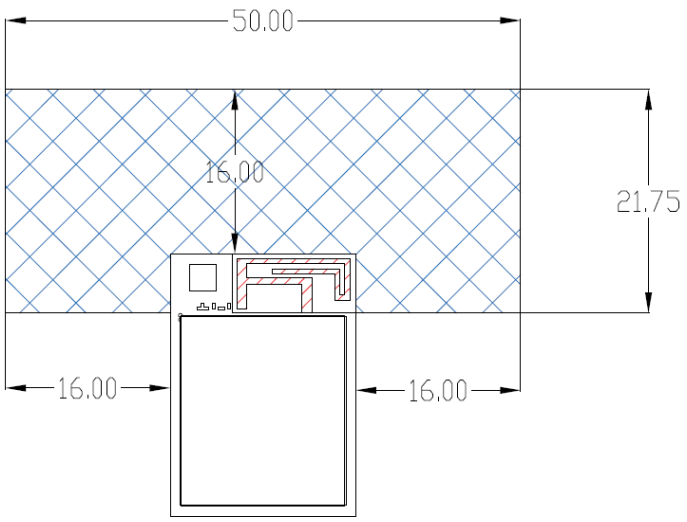


Figure 20: Keepout Area on Motherboard

During PCB design, do not route traces across the RF test point at the bottom of the module to ensure the module performance. The prohibited area during routing is shown in the red box below:

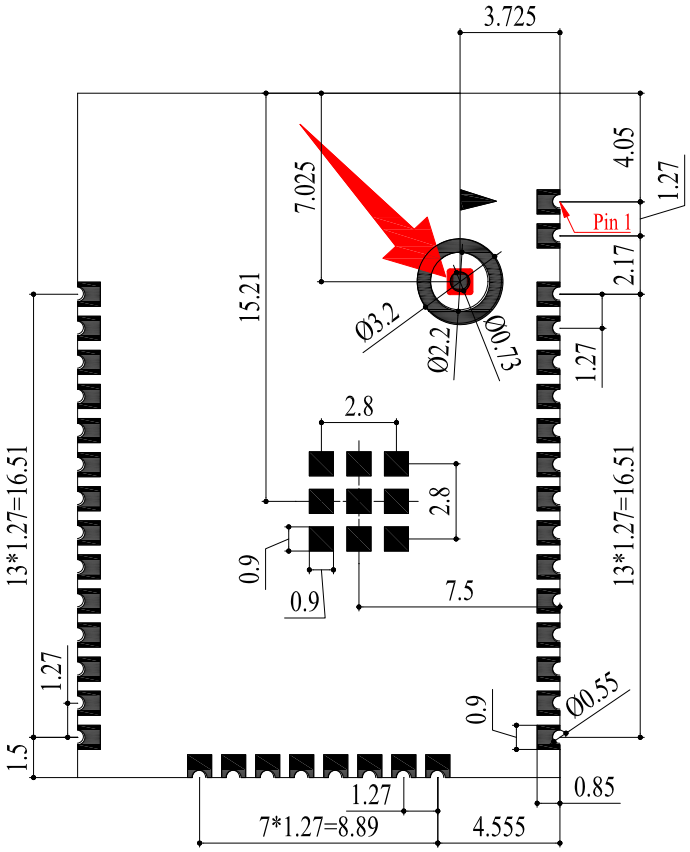


Figure 21: Prohibited Area for Routing

5.3.3. RF Coaxial Connector

5.3.3.1. Receptacle Specifications

The mechanical dimensions of the receptacle supported by the module are as follows.

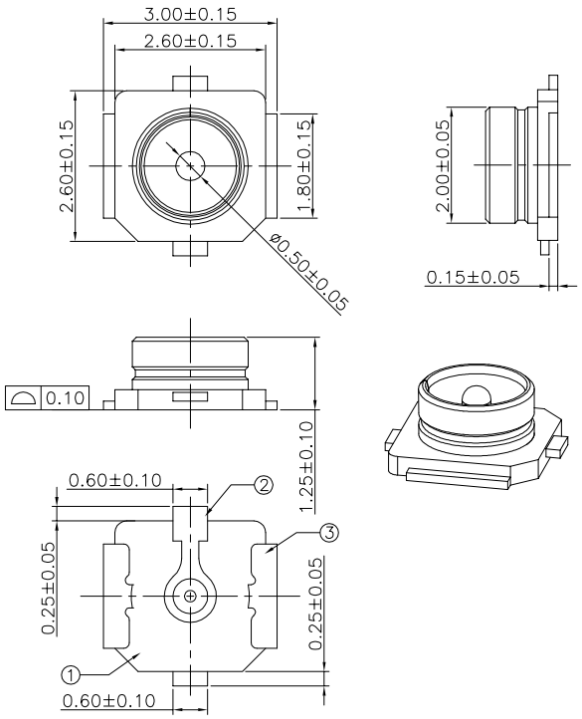


Figure 22: Dimensions of the Receptacle (Unit: mm)

Table 24: Major Specifications of the RF Connector

Item	Specification
Nominal Frequency Range	DC to 6 GHz
Nominal Impedance	50 Ω
Temperature Rating	-40 °C to +85 °C
Voltage Standing Wave Ratio (VSWR)	Meet the requirements of: Max. 1.3 (DC–3 GHz) Max. 1.45 (3–6 GHz)

The RF plug matched with the module antenna base supports the following types and specifications:

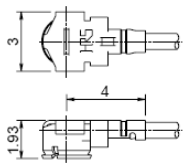
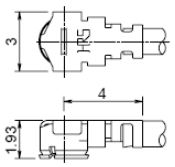
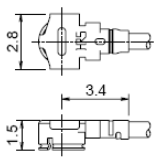
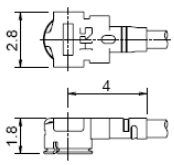
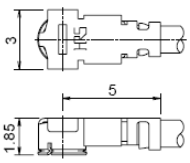
Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 23: Plug specifications matching the antenna base (unit: mm)

The following figure shows the dimensions of the antenna base and plug after assembly:

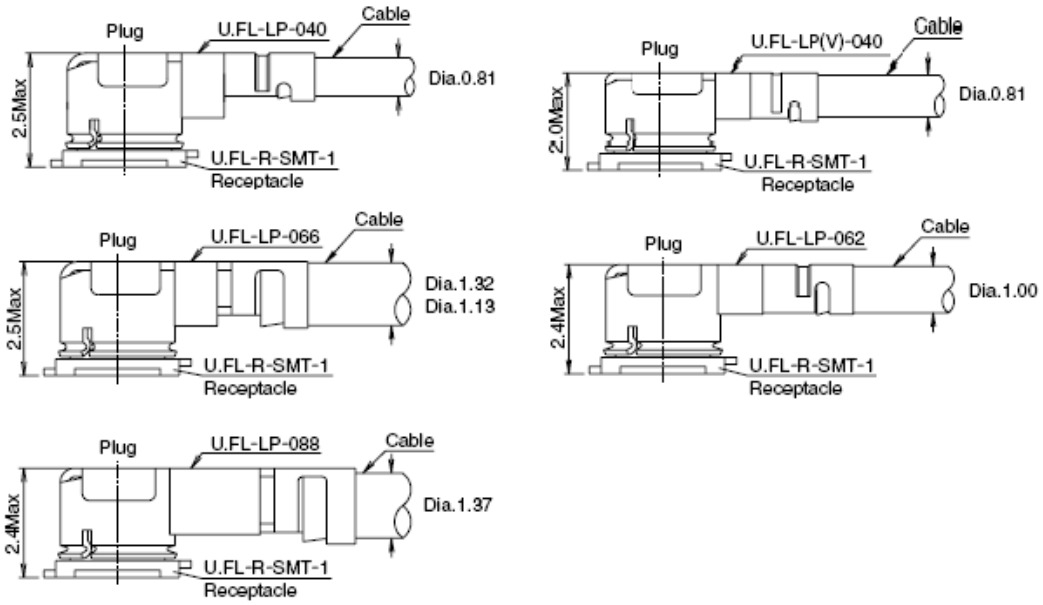


Figure 24: Installation diagram of RF connector (unit: mm)

For more details, please visit https://www.hirose.com.

5.3.3.2. Recommended RF Connector Installation

The pictures for plugging in a coaxial cable plug is shown below, θ = 90° is acceptable, while θ ≠ 90° is not.

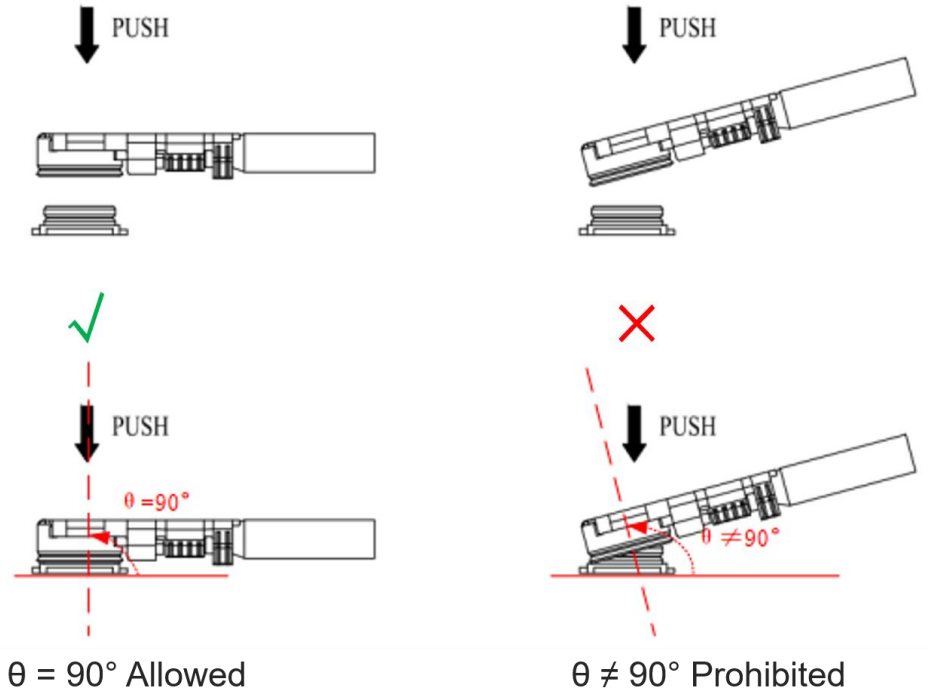


Figure 25: Plug in a Coaxial Cable Plug

The pictures of pulling out the coaxial cable plug is shown below, θ = 90° is acceptable, while θ ≠ 90° is not.

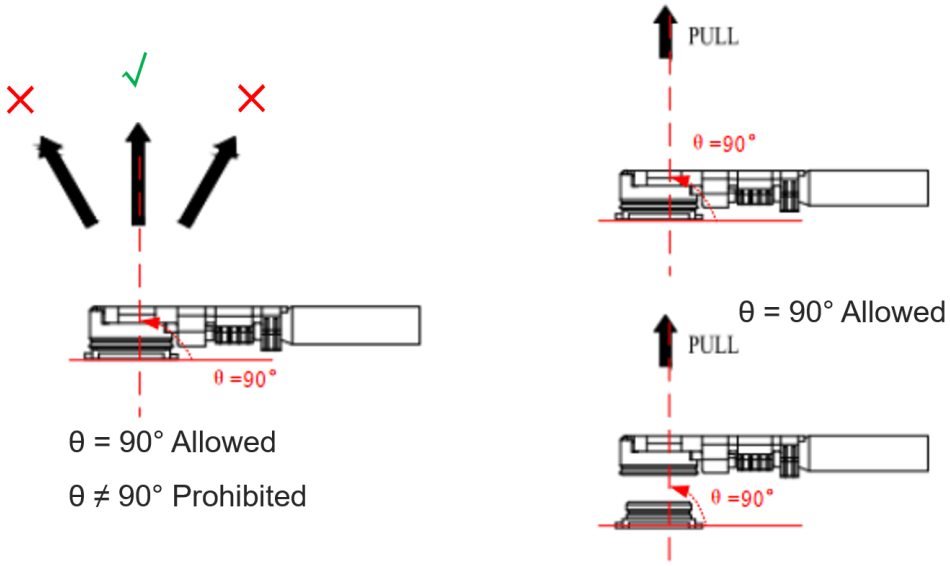


Figure 26: Pull out a Coaxial Cable Plug

The pictures of installing the coaxial cable plug with a jig is shown below, θ = 90° is acceptable, while θ ≠ 90° is not.

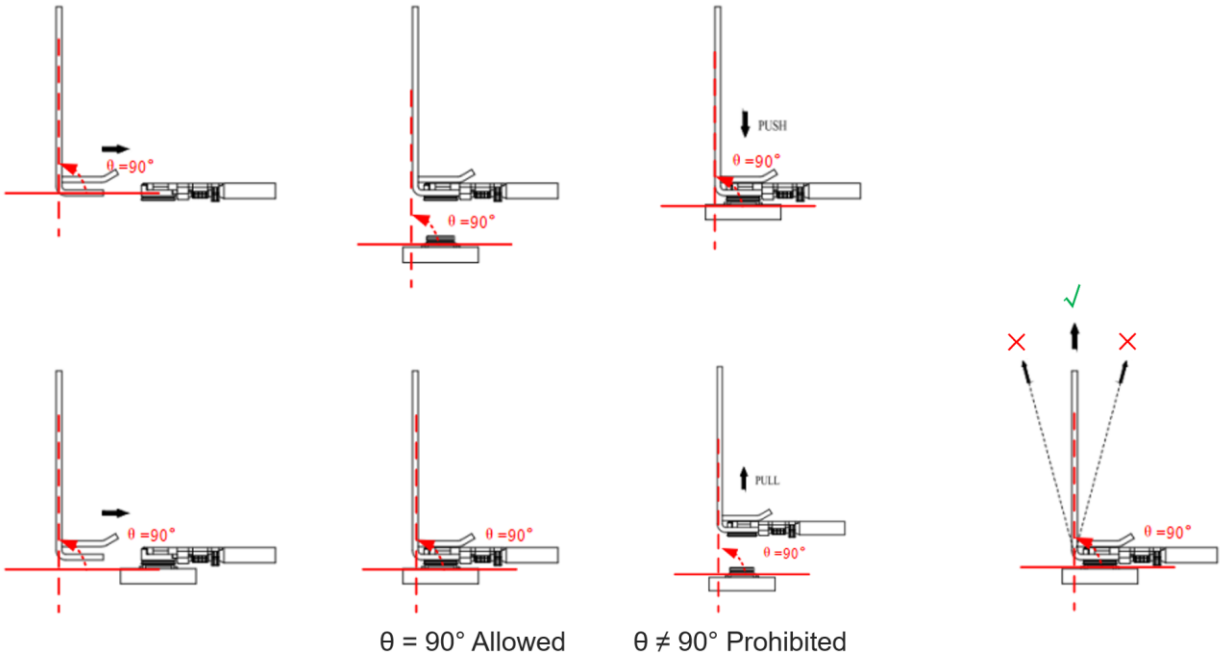


Figure 27: Install the Coaxial Cable Plug with Jig

5.3.3.3. Recommended Manufacturers of RF Connector and Cable

RF connectors and cables by I-PEX are recommended. For more details, visit https://www.i-pex.com.

6 Electrical Characteristics & Reliability

6.1. Absolute Maximum Ratings

Table 25: Absolute Maximum Ratings (Unit: V)

Parameter	Min.	Max.
VBAT	-0.3	3.6
Voltage at Digital Pins	-0.3	3.6
Voltage at ADC[0:1]	0	1.2

6.2. Power Supply Ratings

Table 26: Module Power Supply Ratings (Unit: V)

Parameter	Description	Condition	Min.	Typ.	Max.
VBAT	Power supply for the module	The actual input voltages must be kept between the minimum and maximum values.	3.0	3.3	3.6

6.3. Power Consumption

6.3.1. Wi-Fi Power Consumption [6]

Table 27: Wi-Fi Power Consumption in Non-signaling Mode (Unit: mA)

Condition			I_{VBAT}
2.4 GHz	802.11b	Tx 1 Mbps @ 18 dBm	305.69
		Tx 11 Mbps @ 18 dBm	162.33
	802.11g	Tx 6 Mbps @ 18 dBm	307.33
		Tx 54 Mbps @ 15 dBm	86.23
	802.11n	Tx HT20 MCS 0 @ 18 dBm	310.85
		Tx HT20 MCS 7 @ 15 dBm	126.62
		Tx HT40 MCS 0 @ 18 dBm	314.48
		Tx HT40 MCS 7 @ 15 dBm	128.53
	802.11ax	Tx HE20 MCS 0 @18 dBm	309.74
		Tx HE20 MCS 11 @ 13 dBm	94.83
		Tx HE40 MCS 0 @ 18 dBm	314.55
		Tx HE40 MCS 11 @ 13 dBm	97.10
5 GHz	802.11a	Tx 6 Mbps @ 18 dBm	380.57
		Tx 54 Mbps @ 15 dBm	109.65
	802.11n	Tx HT20 MCS 0 @ 18 dBm	394.82
		Tx HT20 MCS 7 @ 15 dBm	163.34
		Tx HT40 MCS 0 @ 18 dBm	406.76
		Tx HT40 MCS 7 @ 15 dBm	165.96
	802.11ac	Tx VHT20 MCS 0 @ 18 dBm	398.58

[6] The Bluetooth function is disabled when the Wi-Fi power consumption is tested.

		Tx VHT20 MCS 8 @ 14 dBm	140.62
		Tx VHT40 MCS 0 @ 18 dBm	402.03
		Tx VHT40 MCS 9 @ 14 dBm	138.83
	802.11ax	Tx HE20 MCS 0 @ 18 dBm	395.49
		Tx HE20 MCS 11 @ 12 dBm	114.56
		Tx HE40 MCS 0 @ 18 dBm	402.48
		Tx HE40 MCS 11 @ 12 dBm	117.75

6.3.2. Bluetooth Power Consumption [7]

Table 28: Bluetooth Power Consumption in Non-signaling Mode (Unit: mA)

Condition	I_{VBAT}
BR @ 2.96 dBm	97.57
EDR (π/4-DQPSK) @ 0.83 dBm	94.66
EDR (8-DPSK) @ 0.84 dBm	94.55
BLE (1 Mbps) @ 3.73 dBm	107.14
BLE (2 Mbps) @ 3.75 dBm	78.22

6.4. Digital I/O Characteristics

Table 29: VBAT I/O Requirements (Unit: V)

Parameter	Description	Min.	Max.
V_{IH}	High-level Input Voltage	0.7 × VBAT	VBAT
V_{IL}	Low-level Input Voltage	0	0.3 × VBAT

[7] The Wi-Fi function is disabled when the Bluetooth power consumption is tested.

V_{OH}	High-level Output Voltage	0.9 × VBAT	VBAT
V_{OL}	Low-level Output Voltage	-0	0.1 × VBAT

6.5. ESD Protection

Static electricity occurs naturally and may damage the module. Therefore, applying proper ESD countermeasures and handling methods is imperative. For example, wear anti-static gloves during the development, production, assembly and testing of the module; add ESD protection components to the ESD sensitive interfaces and points in the product design.

Table 30: ESD Characteristics (Unit: kV)

Model	Test Result	Standard
Human Body Model (HBM)	±3	*ANSI/ESDA/JEDEC JS-001-2017*
Charged Device Model (CDM)	±0.35	*ANSI/ESDA/JEDEC JS-002-2018*

7 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeters (mm), and the dimensional tolerances are ±0.2 mm unless otherwise specified.

7.1. Mechanical Dimensions

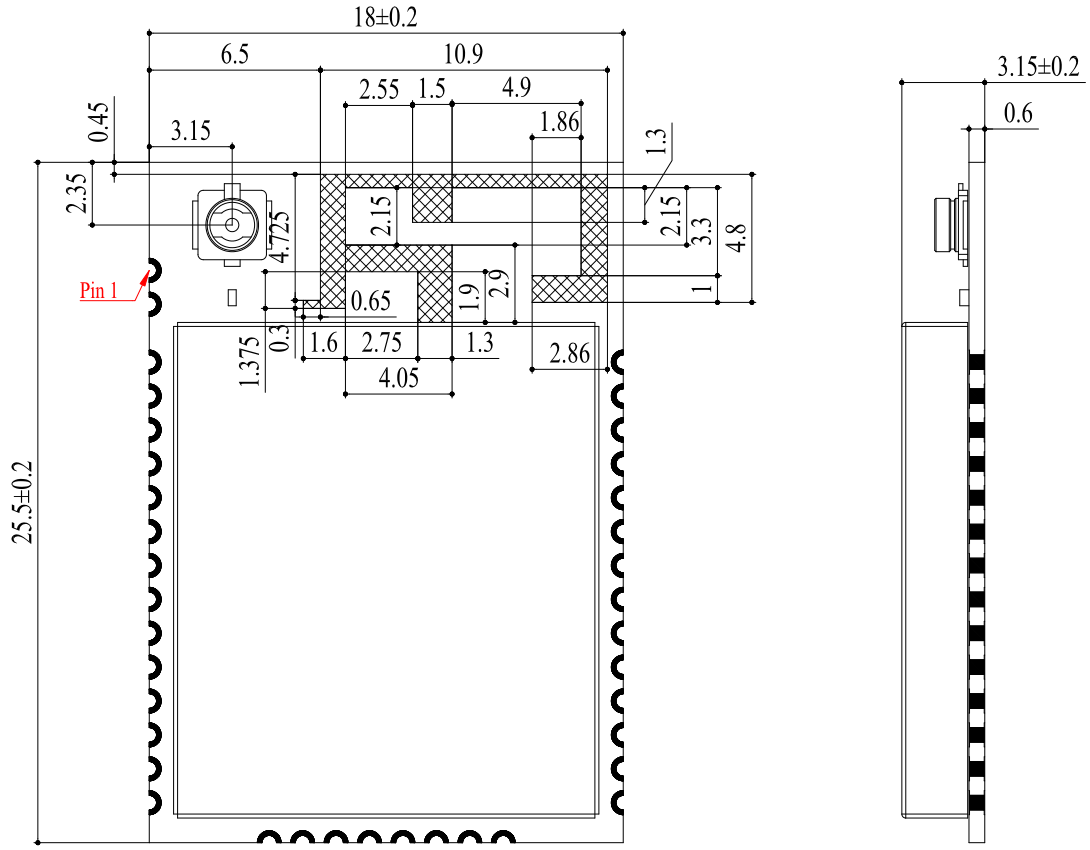


Figure 28: Top and Side Dimensions

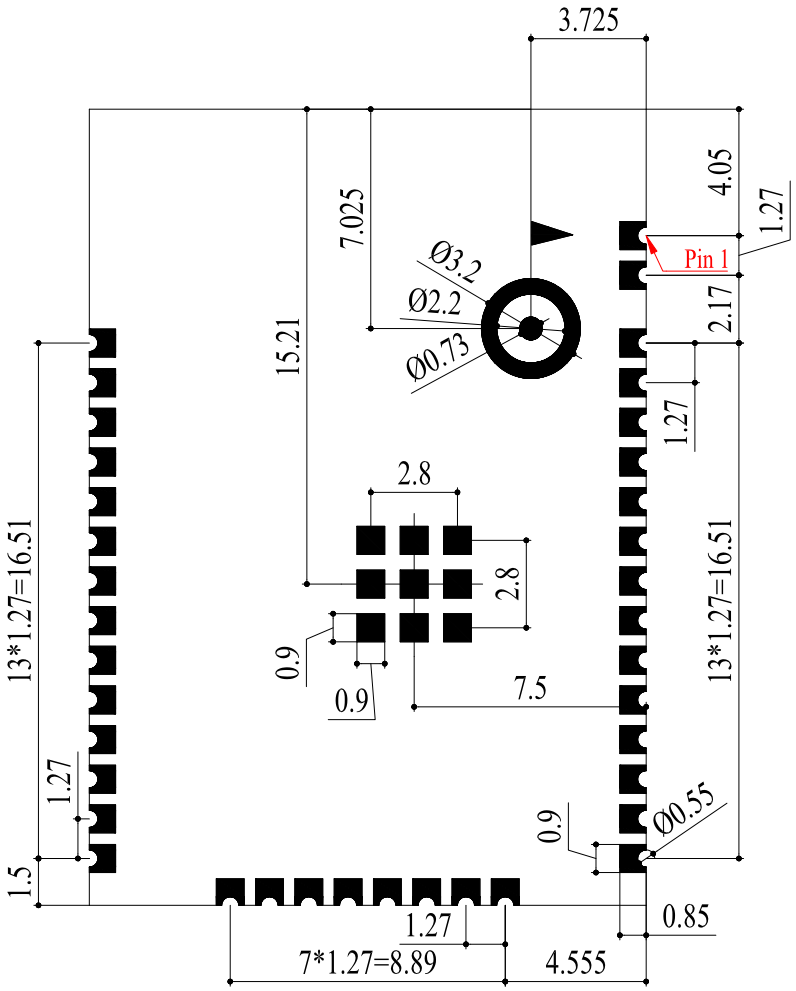


Figure 29: Bottom Dimensions (Bottom View)

NOTE

The package warpage level of the module refers to the *JEITA ED-7306* standard.

7.2. Recommended Footprint

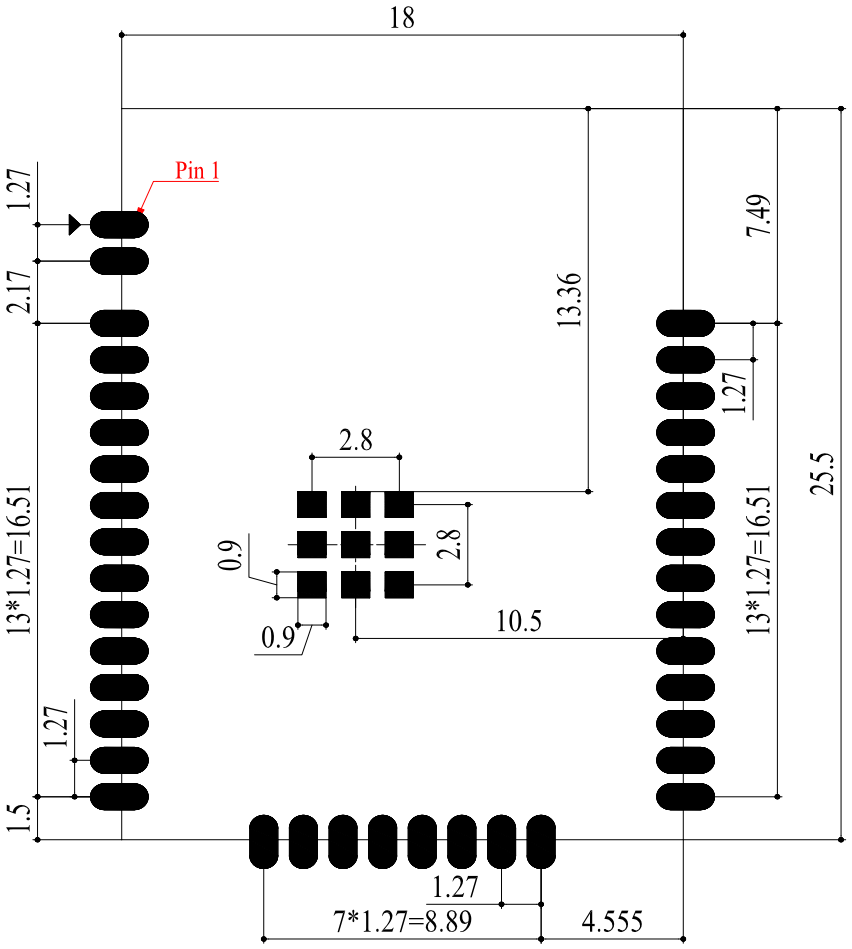


Figure 30: Recommended Footprint

NOTE

Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.

7.3. Top and Bottom Views

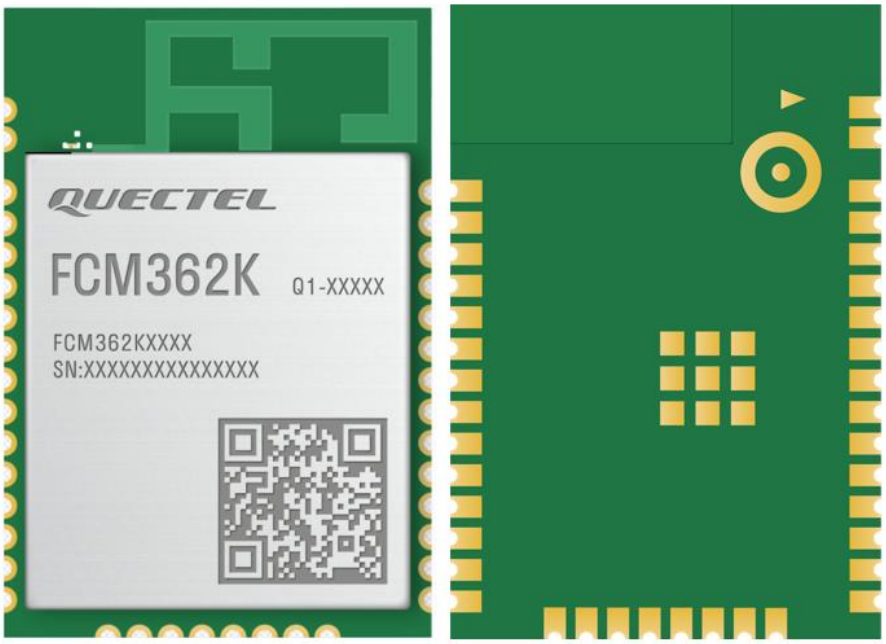


Figure 31: Top and Bottom Views (Pin Antenna Interface)

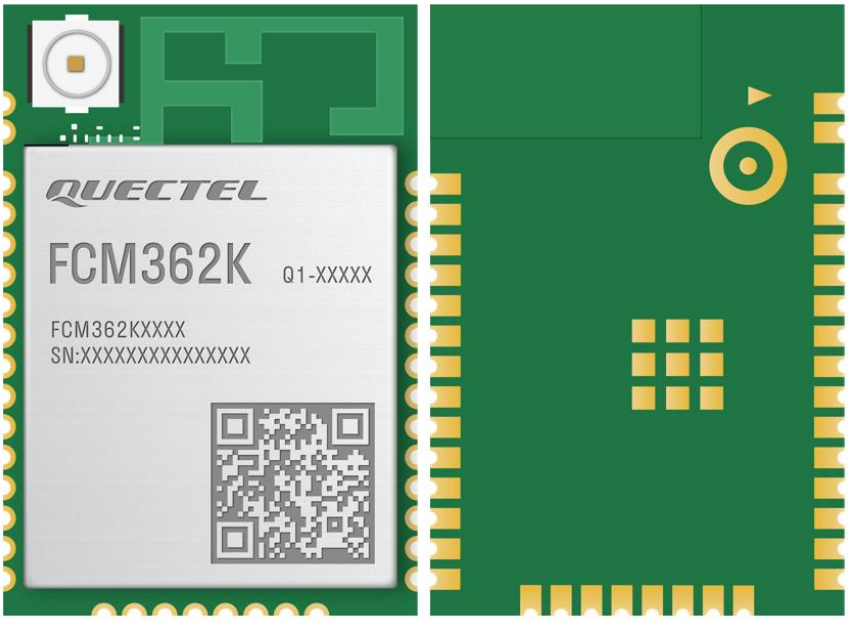


Figure 32: Top and Bottom Views (RF Coaxial Connector)

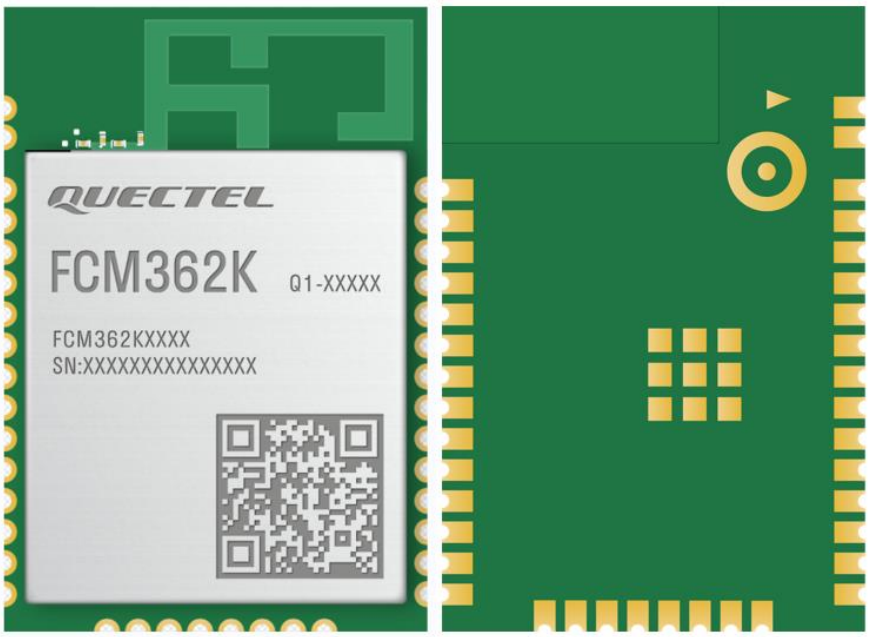


Figure 33: Top and Bottom Views (PCB Antenna Interface)

NOTE

1. Images above are for illustrative purposes only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Quectel.
2. The RF coaxial connector is not soldered when the module is designed with pin antenna interface (ANT_WIFI/BT) or a PCB antenna.

8 Storage, Manufacturing & Packaging

8.1. Storage Conditions

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: the temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.

2. Shelf life (in a vacuum-sealed packaging): 12 months in Recommended Storage Condition.

3. Floor life: 168 hours [8] in a factory where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g., a dry cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement mentioned above;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 8 hours at 120 ±5 °C;
   - The module must be soldered to PCB within 24 hours after the baking, otherwise it should be put in a dry environment such as in a dry cabinet.

[8] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. And do not unpack the modules in large quantities until they are ready for soldering.

NOTE

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

8.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To guarantee module soldering quality, the thickness of stencil for the module is recommended to be 0.15–0.18 mm. For more details, see ***document [3]***.

The recommended peak reflow temperature should be 235–246 ºC, with 246 ºC as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is recommended that the module should be mounted only after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

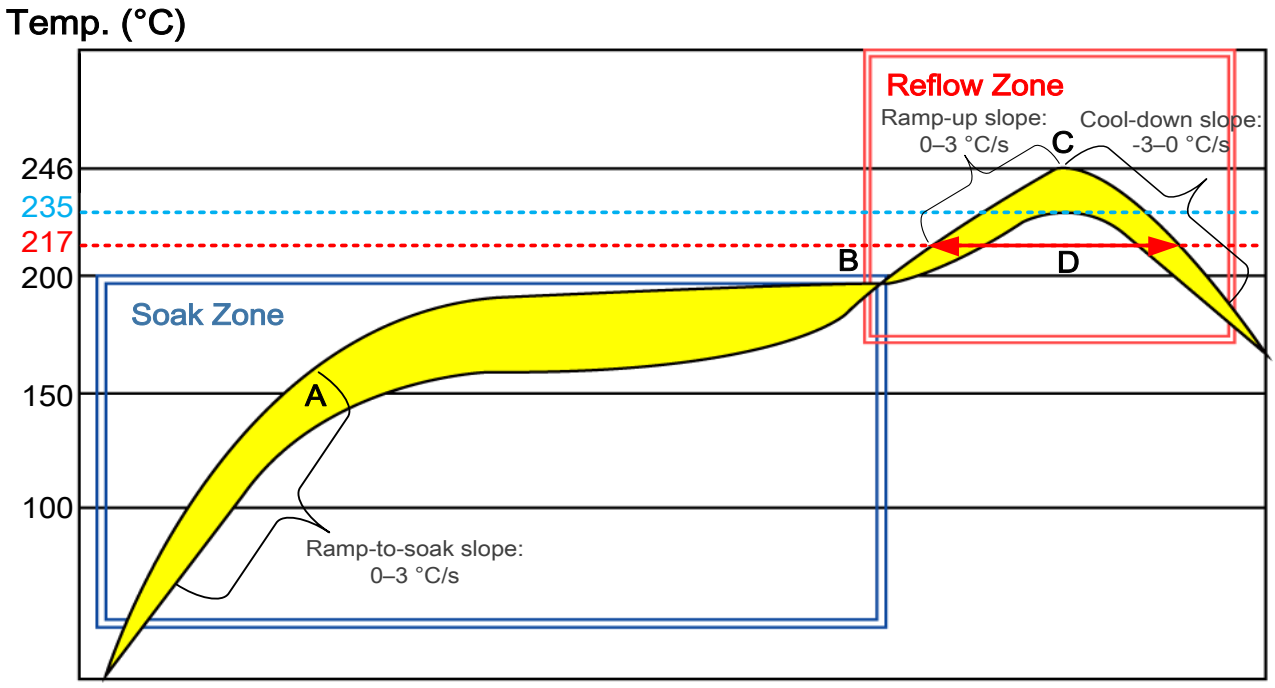


Figure 34: Recommended Reflow Soldering Thermal Profile

Table 31: Recommended Thermal Profile Parameters

Factor	Recommended Value
Soak Zone	
Ramp-to-soak slope	0–3 °C/s
Soak time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
Ramp-up slope	0–3 °C/s
Reflow time (D: over 217 °C)	40–70 s
Max. temperature	235–246 °C
Cool-down slope	-3–0 °C/s
Reflow Cycle	
Max. reflow cycle	1

NOTE

1. The above profile parameter requirements are for the measured temperature of solder joints. Both the hottest and coldest spots of solder joints on the PCB should meet the above requirements.
2. During manufacturing and soldering, or any other processes that may contact the module directly, NEVER wipe the module's shielding can with organic solvents, such as acetone, ethyl alcohol, isopropyl alcohol, trichloroethylene, etc. Otherwise, the shielding can may become rusted.
3. The shielding can for the module is made of Cupro-Nickel base material. It is tested that after 12 hours' Neutral Salt Spray test, the laser engraved label information on the shielding can is still clearly identifiable and the QR code is still readable, although white rust may be found.
4. If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
5. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
6. Avoid using materials that contain mercury (Hg), such as adhesives, for module processing, even if the materials are RoHS compliant and their mercury content is below 1000 ppm (0.1 %).
7. Due to the complexity of the SMT process, please contact Quectel Technical Support in advance for any situation that you are not sure about, or any process (e.g. selective soldering, ultrasonic soldering) that is not mentioned in ***document [3]***.

8.3. Packaging Specification

This chapter outlines the key packaging parameters and processes. All figures below are for reference purposes only, as the actual appearance and structure of packaging materials may vary in delivery.

The modules are packed in a tape and reel packaging as specified in the sub-chapters below.

8.3.1. Carrier Tape

Carrier tape dimensions are illustrated in the following figure and table:

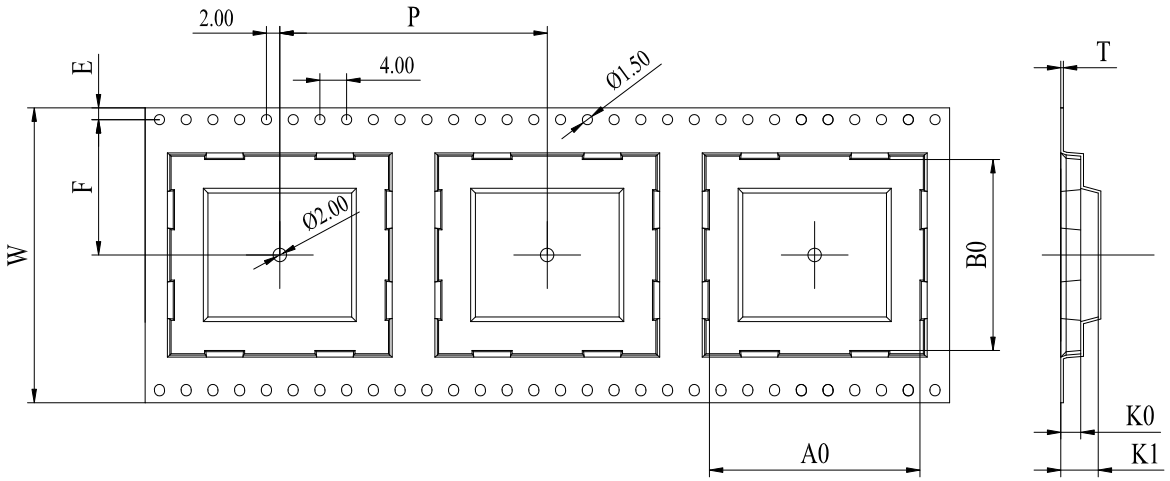


Figure 35: Carrier Tape Dimension Drawing (Unit: mm)

Table 32: Carrier Tape Dimension Table (Unit: mm)

W	P	T	A0	B0	K0	K1	F	E
44	32	0.4	18.4	25.9	3.7	6.8	20.2	1.75

8.3.2. Plastic Reel

Plastic reel dimensions are illustrated in the following figure and table:

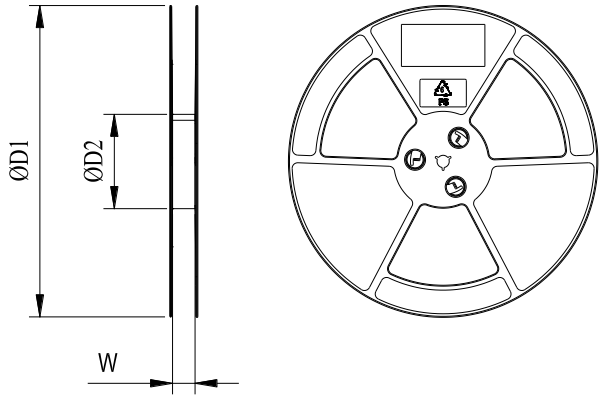


Figure 36: Plastic Reel Dimension Drawing

Table 33: Plastic Reel Dimension Table (Unit: mm)

øD1	øD2	W
330	100	44.5

8.3.3. Mounting Direction

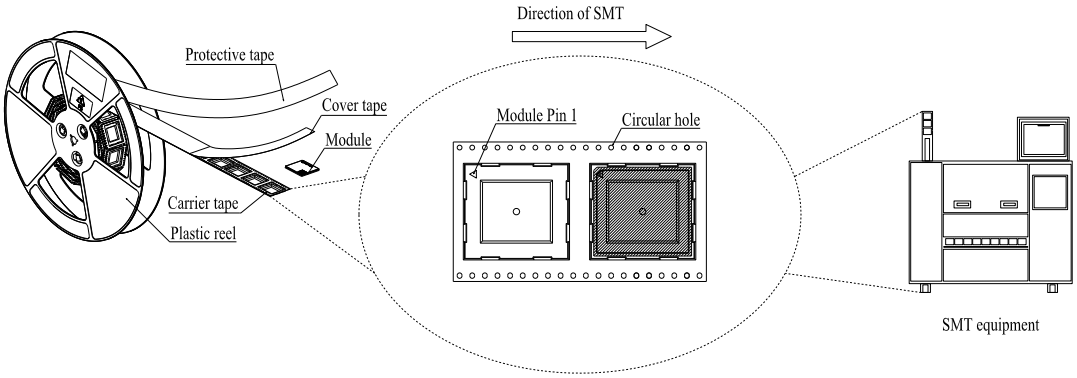
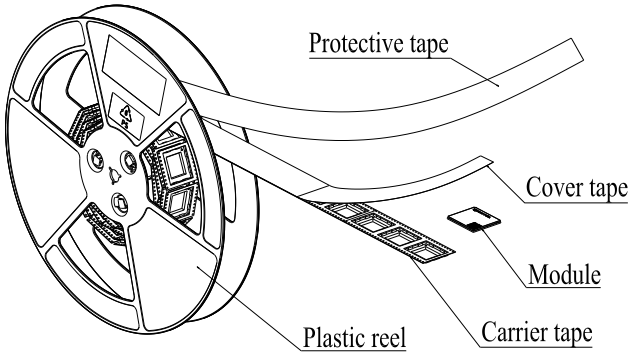


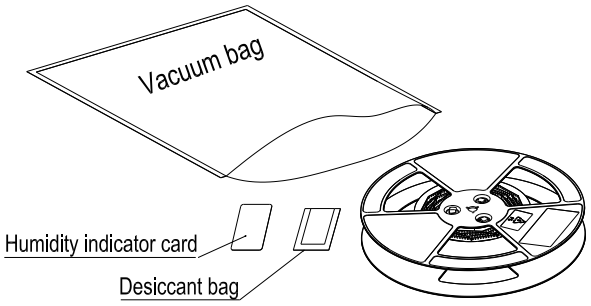
Figure 37: Mounting Direction

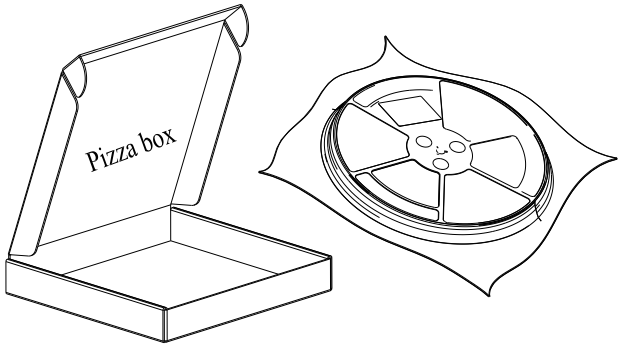
8.3.4. Packaging Process



Place the modules onto the carrier tape cavity and cover them securely with cover tape. Wind the heat-sealed carrier tape onto a plastic reel and apply a protective tape for additional protection. 1 plastic reel can pack 250 modules.

Place the packaged plastic reel, humidity indicator card and desiccant bag into a vacuum bag, and vacuumize it.





Place the vacuum-packed plastic reel into a pizza box.

Place the 4 packaged pizza boxes into 1 carton and seal it. 1 carton can pack 1000 modules.

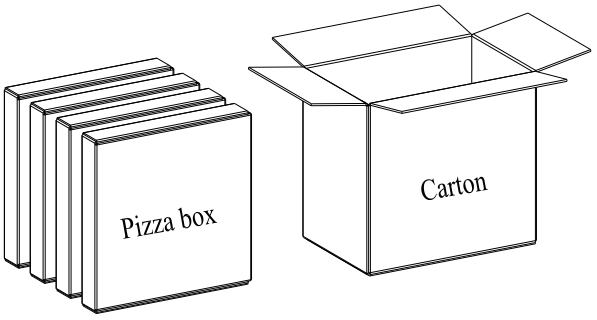


Figure 38: Packaging Process

9 Appendix References

Table 34: Reference Documents

Document Name
[1] Quectel_FCM362K_TE-B_User_Guide
[2] Quectel_RF_Layout_Application_Note
[3] Quectel_Module_SMT_Application_Note

Table 35: Terms and Abbreviations

Abbreviation	Description
ADC	Analog-to-Digital Converter
AMBA	Advanced Microcontroller Bus Architecture
AP	Access Point
APB	Advanced Peripheral Bus
BLE	Bluetooth Low Energy
BPSK	Binary Phase Shift Keying
CCK	Complementary Code Keying
CDM	Charged Device Model
DMA	Direct Memory Access
DPSK	Differential Phase Shift Keying
DQPSK	Differential Quadrature Reference Phase Shift Keying
ESD	Electrostatic Discharge
EVM	Error Vector Magnitude

GFSK	Gauss frequency Shift Keying
GND	Ground
GPIO	General-Purpose Input/Output
HBM	Human Body Model
HT	High Throughput
I/O	Input/Output
I2C	Inter-Integrated Circuit
I2S	Inter-IC Sound
IEEE	Institute of Electrical and Electronics Engineers
kbps	Kilobits Per Second
LCC	Leadless Chip Carrier (package)
Mbps	Million Bits Per Second
MCU	Microcontroller Unit
MFP	Management Frame Protection
OTA	Over The Air
PCB	Printed Circuit Board
PCM	Pulse Code Modulation
PWM	Pulse Width Modulation
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RoHS	Restriction of Hazardous Substances
ROM	Read Only Memory
RTC	Real Time Clock
SAE	Simultaneous Authentication of Equals
SD	Secure Digital
SDIO	Secure Digital Input/Output

SMD	Surface Mount Device
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
STA	Station
TBD	To Be Determined
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
(U)SIM	(Universal) Subscriber Identity Module
V_{IH}	High-level Input Voltage
V_{IL}	Low-level Input Voltage
Vmax	Maximum Voltage
Vmin	Minimum Voltage
Vnom	Normal Voltage Value
V_{OH}	High-level Output Voltage
V_{OL}	Low-level Output Voltage
VSWR	Voltage Standing Wave Ratio
WEP	Wired Equivalent Privacy
Wi-Fi	Wireless Fidelity
WPA	Wi-Fi Protected Access