SC66 Display Driver Development Guide

Smart Module Series

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About the Document

History

Revision	Date	Author	Description
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1 Introduction

This document describes how to use the Display Serial Interface (DSI) to bring up the display panel on the Android platform of Quectel SC66 module.

This document only describes the important parts of display driver development.

NOTE

In this document, Smart EVB G2's LCD HX8394F is used as an example.

2 XML Tags from GCDB for Panel Configuration

The Global Component Database (GCDB) parser provides configuration options for the display panel on SDM660 chipset.

This chapter describes the display XML tags required to configure the Android kernel and the little kernel (LK) to bring up the panel. The following sections provide detailed information on input entries, descriptions and possible values of the XML tags that can be used in the display parser module for the GCDB, version 1.0.

NOTE

This document only describes the important parameters. The unspecified parameters usually do not need to be modified.

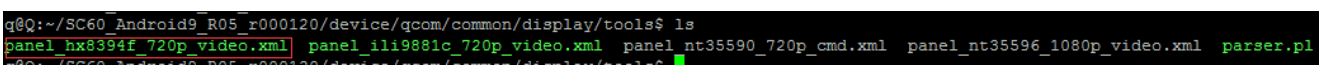
2.1. Display Driver Development Procedure

Take the following steps to develop display driver for any display panel and platform. The procedure can also be found at *device/qcom/common/display/tools/README.txt*.

1. Install the libraries by the following commands.

```
#sudo apt-get install libxml-libxml-perl
#sudo apt-get install libxml-perl
```

2. Enter the tools directory *#cd device/qcom/common/display/tools*, the following information will appear.



3. Copy a new .XML file to edit.

- If the LCD is in video mode, copy the *panel_nt35596_1080p_video.xml* to a new *<oem_panel_input_file>.xml*.
- If the LCD is in command mode, copy the *panel_nt35590_720p_cmd.xml* to a new *<oem_panel_input_file>.xml*.

Taking HX8394F as an example, the new .XML file will be:

```
#cp panel_nt35596_1080p_video.xml panel_hx8394f_720p_video.xml
```

NOTE

In most cases, LCD is in video mode which is determined by the LCD module type.

4. Edit the new .XML to configure the display parameters.

```
<GCDB>
  <Version>"1.0"</Version>
  <PanelId>hx8394f-720p-video</PanelId>
  <PanelH>hx8394f_720p_video</PanelH>
  <PanelEntry>

    <!-- Panel configuration -->
    <PanelName>"hx8394f 720p video mode dsi panel"</PanelName>
    <PanelController>"mdss_dsi0"</PanelController>
    <PanelInterface>10</PanelInterface>
```

The configuration details are present at ***Chapters 2.2~2.8***.

5. Generate the device tree file (.dtsi) and header file (.h) by executing the following command:

```
#perl parser.pl <oem_panel_input_file>.xml panel
```

Taking HX8394F as an example, the command will be:

```
#perl parser.pl panel_hx8394f_720p_video.xml panel
```

By executing this command, *dsi-panel-hx8394f-720p-video.dtsi* and *panel_hx8394f_720p_video.h* will be generated.

6. Copy .dtsi to dts folder by executing the following command:

```
#cp device/qcom/common/display/tools/dsi-panel-hx8394f-720p-video.dtsi
     kernel/msm-4.4/arch/arm64/boot/dts/qcom/
```

7. Configure the Android kernel (see ***Chapter 3*** for details).

8. Build image by executing the following commands:

```
source build/envsetup.sh
lunch sdm660_64-userdebug
make bootimage
```

Then users will get *boot.img* in the directory *out/target/product/sdm660_64/.*

2.2. Tags for Panel Configuration

This chapter defines the specific XML tag entries for the panel.

File path: *device/qcom/common/display/tools/<oem_panel_input_file>.xml*

2.2.1. Panel Information

The parser expects the entries in the following table to be part of the **<GCDB>** XML tag.

Table 1: Panel Information

XML Tag/Entry	Description	Value
Version	Each version is bind to be a set of panel tags.	MAJOR_VERSION.MINOR_VERSION For example: in 1.0, 1 means the major version and 0 means the minor version.
PanelId	Name used to generate the *.dtsi* file for kernel.	See the following XML input example.
PanelH	Name used to generate the header file for LK.	See the following XML input example.

For example:

```
<GCDB>
  <Version>"1.0"</Version>
  <PanelId>hx8394f-720p-video</PanelId>
  <PanelH>hx8394f_720p_video</PanelH>
  <PanelEntry>
```

2.2.2. Panel Configuration Information

The parser expects all other entries to be part of the **<GCDB>** and **<PanelEntry>** tag. Please refer to the following XML input example for more information.

Table 2: Panel Configuration

XML Tag/Entry	Description	Value
PanelName	Panel name	Name/label value
PanelType	Panel is in video mode or command mode.	0 = video mode 1 = command mode
PanelOrientation (Only used in LK)	Panel rotation value. If this entry is not mentioned, LK will be configured with default 0 degree rotation.	1 = 0 degree 2 = 180 degrees
PanelFrameRate	An integer to define the panel refresh rate per second.	For example: 60 for 60fps panel.

For example:

```
<!-- Panel configuration -->
<PanelName>"hx8394f 720p video mode dsi panel"</PanelName>
<PanelController>"mdss_dsi0"</PanelController>
<PanelInterface>10</PanelInterface>
<PanelType>0</PanelType>
<PanelDestination>"DISPLAY_1"</PanelDestination>
<PanelOrientation>0</PanelOrientation>
<PanelFrameRate>60</PanelFrameRate>
<PanelChannelId>0</PanelChannelId>
<DSIVirtualChannelId>0</DSIVirtualChannelId>
<PanelBroadcastMode>0</PanelBroadcastMode>
<!-- Optional Panel configuration -->
<!--BitClockFrequency>0</BitClockFrequency -->
<DSIStream>0</DSIStream>
<PanelCompatible>"qcom,mdss-dsi-panel"</PanelCompatible>
<InterleaveMode>0</InterleaveMode>
```

2.2.3. Panel Resolution

The following table defines different panel resolution-specific tags. All dimensions should be provided in pixel format.

Table 3: Panel Resolution Configuration

XML Tag/Entry	Description
PanelWidth	Panel width
PanelHeight	Panel height
HFrontPorch	Horizontal front porch value
HBackPorch	Horizontal back porch value
HPulseWidth	Horizontal pulse width
HSyncSkew	Horizontal sync skew value
VBackPorch	Vertical back porch value
VFrontPorch	Vertical front porch value
VPulseWidth	Vertical pulse width

For example:

```
<!-- Panel Resolution -->
<PanelWidth>720</PanelWidth>
<PanelHeight>1280</PanelHeight>
<HFrontPorch>50</HFrontPorch>
<HBackPorch>50</HBackPorch>
<HPulseWidth>50</HPulseWidth>
<HSyncSkew>0</HSyncSkew>
<VBackPorch>20</VBackPorch>
<VFrontPorch>8</VFrontPorch>
<VPulseWidth>4</VPulseWidth>
<HLeftBorder>0</HLeftBorder>
<HRightBorder>0</HRightBorder>
<VTopBorder>0</VTopBorder>
<VBottomBorder>0</VBottomBorder>
<!-- Optional Panel resolution configuration -->
<!--HActiveRes>0</HActiveRes>
<VActiveRes>100</VActiveRes>
<InvertDataPolarity>0</InvertDataPolarity>
<InvertVsyncPolarity>0</InvertVsyncPolarity>
<InvertHsyncPolarity>0</InvertHsyncPolarity -->
```

2.2.4. Panel Color Information

The panel color information includes color format, swap values, and border color, some of which are defined in the following table.

Table 4: Panel Color Information

XML Tag/Entry	Description	Value
ColorFormat	Defines the bits per pixel.	24 = 888_RGB 18 = 666_RGB 16 = 565_RGB 12 = 444_RGB 8 = 332_RGB 3 = 111_RGB
ColorOrder	Defines pixel component color order between MSM and panel.	0 = DSI_RGB_SWAP_RGB 1 = DSI_RGB_SWAP_RBG 2 = DSI_RGB_SWAP_BGR 3 = DSI_RGB_SWAP_BRG 4 = DSI_RGB_SWAP_GRB 5 = DSI_RGB_SWAP_GBR

For example:

```
<!-- Panel Color Information -->
<ColorFormat>24</ColorFormat>
<ColorOrder>0</ColorOrder>
<UnderFlowColor>0xff</UnderFlowColor>
<BorderColor>0</BorderColor>
```

2.3. Panel Command Information

This chapter describes the on/off commands sent to the panel. Users can send all valid DSI commands to the panel.

Table 5: Panel Command Information

XML Tag/Entry	Description	Value
OnCommand	Array of variable length that lists the initialization commands of the panel.	See ***Chapter 2.3.1***
OffCommand	Array of variable length that lists the deinitialization commands of the panel.	
OnCommandState	Panel state when sending the on command.	0 = DSI_LP_MODE 1 = DSI_HP_MODE
OffCommandState	Panel state when sending the off command.	

Generally speaking, **<OnCommandState>** and **<OffCommandState>** only need to keep the default values.

```
<!-- Panel Command information -->
<OnCommand>"0x39, 0x01, 0x00, 0x00, 0x00, 0x00, 0x04, 0xFF, 0x98, 0x81, 0x03,
0x39, 0x01, 0x00, 0x00, 0x00, 0x00, 0x02, 0x01, 0x00,
0x39, 0x01, 0x00, 0x00, 0x00, 0x00, 0x02, 0x02, 0x00,
```

```
<OffCommand>"0x05, 0x01, 0x00, 0x00, 0x32, 0x00, 0x02, 0x28, 0x00,
             0x05, 0x01, 0x00, 0x00, 0x78, 0x00, 0x02, 0x10, 0x00"</OffCommand>
<OnCommandState>0</OnCommandState>
<OffCommandState>1</OffCommandState>
```

2.3.1. Command Format

Each command needs the input information listed in the following table. The current parser supports one complete command per line.

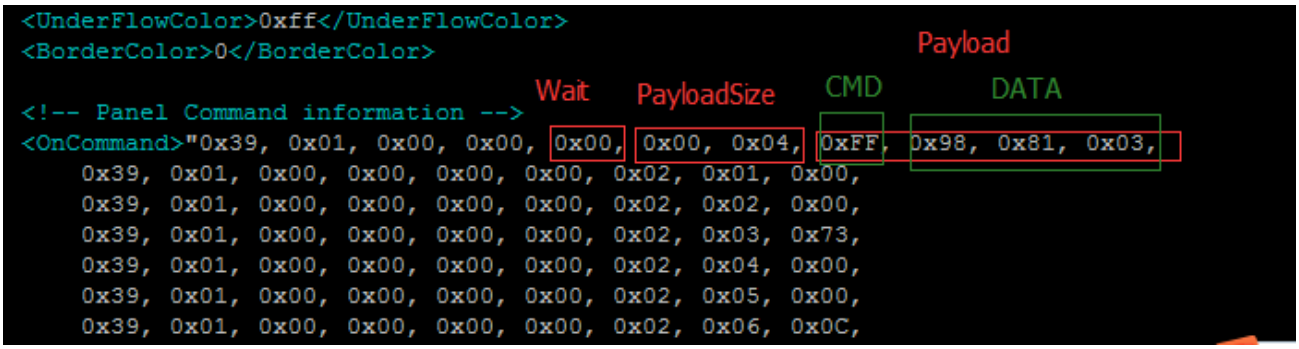
Table 6: Command Format

Subentry	Description	Byte Length
CommandType	Data type of command	1
Last	Specifies if this command packet is individual or not.	1
VC	Virtual channel used to send this command.	1
ACK	Needs acknowledgement from the panel.	1
Wait	Sleep in milliseconds before sending next command.	1
PayloadSize	Payload size	2
Payload	Actual command	Based on PayloadSize

1. Usually, only “PayloadSize” and “Payload” need to be modified.

Some LCD may need to wait for several milliseconds before sending the next command. Then the parameter “Wait” need to be modified.

For example:



2. Parameter “Payload” is provided by the LCD module manufacturer.

The parameters provided by LCD module manufacturer in the following format are preferable:

```
REGISTER, CMD(Hex), Number(Hex), DATA(Hex), DATA(Hex), …
```

When parameters are provided in the above formats, the **<OnCommand>** parameters will be:

```
0x39, 0x01, 0x00, 0x00, 0x00 = REGISTER
PayloadSize = Number+1
Payload = CMD,DATA,DATA,…
```

For example, if the parameters provided by LCD module manufacturers are:

```
REGISTER,FF,3,98,81,03
REGISTER,01,01,00
```

The **<OnCommand>** parameters will be:

```
0x39, 0x01, 0x00, 0x00, 0x00, 0x00, 0x04, 0xFF, 0x98, 0x81, 0x03,
0x39, 0x01, 0x00, 0x00, 0x00, 0x00, 0x02, 0x01, 0x00,
```

3. Usually the last two commands of **<OnCommand>** are available as shown below, but some LCD chips do not need them.

```
0x05, 0x01, 0x00, 0x00, 0x78, 0x00, 0x02, 0x11, 0x00,
0x05, 0x01, 0x00, 0x00, 0x05, 0x00, 0x02, 0x29, 0x00,
```

```
    0x39, 0x01, 0x00, 0x00, 0x01, 0x00, 0x02, 0x2E, 0x44,
    0x39, 0x01, 0x00, 0x00, 0x01, 0x00, 0x02, 0xE0, 0x00,
    0x05, 0x01, 0x00, 0x00, 0x78, 0x00, 0x02, 0x11, 0x00,
    0x05, 0x01, 0x00, 0x00, 0x05, 0x00, 0x02, 0x29, 0x00"</OnCommand>
<OffCommand>"0x05, 0x01, 0x00, 0x00, 0x32, 0x00, 0x02, 0x28, 0x00,
             0x05, 0x01, 0x00, 0x00, 0x78, 0x00, 0x02, 0x10, 0x00"</OffCommand>
```

0x11: sleep out command of LCD.
0x29: display on command of LCD.

2.4. Video Mode Panel

The following table describes the video mode panel configuration entries.

Table 7: Video Mode Panel

XML Tag/Entry	Description	Value
HSyncPulse	Horizontal synchronization pulses. It determines whether the hardware should send horizontal synchronization pulses during the vertical blanking period.	0 = Synchronization pulse disable 1 = Synchronization pulse enable
TrafficMode	Panel traffic mode type	0 = non burst with synchronization pulses 1 = non burst with synchronization start event 2 = burst mode

Usually, these parameters do not need to be modified. Users may need to note the parameter "TrafficMode" which may vary with the LCD chip. For example:

```
<!-- Video mode panel information -->
<HSyncPulse>1</HSyncPulse>
<HFPPowerMode>0</HFPPowerMode>
<HBPPowerMode>0</HBPPowerMode>
<HSAPowerMode>0</HSAPowerMode>
<BLLPEOFPowerMode>1</BLLPEOFPowerMode>
<BLLPPowerMode>1</BLLPPowerMode>
<TrafficMode>2</TrafficMode>
<DMADelayAfterVsync>0</DMADelayAfterVsync>
<BLLPEOFPower>0x9</BLLPEOFPower>
```

2.5. Lane Configuration

The foloowing table lists the DSI panel's lane configuration entries.

Table 8: Lane Configuration

XML Tag/Entry	Description	Value
DSILanes	Number of lanes used for communication with DSI.	2 for 2 lane panel 4 for 4 lane panel
DSILaneMap	It defines how the data lanes are mapped to the panel.	0 = DLANE_SWAP_0123 1 = DLANE_SWAP_3012 2 = DLANE_SWAP_2301 3 = DLANE_SWAP_1230 4 = DLANE_SWAP_0321 5 = DLANE_SWAP_1032 6 = DLANE_SWAP_2103 7 = DLANE_SWAP_3210
Lane0State	Lane 0 state	1 = ENABLE 0 = DISABLE
Lane1State	Lane 1 state	
Lane2State	Lane 2 state	
Lane3State	Lane 3 state	

For example:

```
<!-- Lane Configuration -->
<DSILanes>4</DSILanes>
<DSILaneMap>0</DSILaneMap>
<Lane0State>1</Lane0State>
<Lane1State>1</Lane1State>
<Lane2State>1</Lane2State>
<Lane3State>1</Lane3State>
```

2.6. Panel Physical Data

The following table describes all panel's physical configuration register entries.

Table 9: Panel Physical Data

XML Tag/Entry	Description	Value
PanelTimings	An array of length 12 that specifies the physical timing settings for the panel	
TClkPost	DSI timing control clock post value	
TClkPre	DSI timing control clock pre-value	

For example:

```
<!-- Panel Timing -->
<PanelTimings>"0x7B, 0x1A, 0x10, 0x00, 0x3C, 0x40, 0x14, 0x1C, 0x15, 0x03, 0x04, 0x00"</PanelTimings>
<DSIMDPTrigger>0</DSIMDPTrigger>
<DSIDMATrigger>4</DSIDMATrigger>
<TClkPost>0x04</TClkPost>
<TClkPre>0x1A</TClkPre>
```

2.6.1. Generate DSI Timing

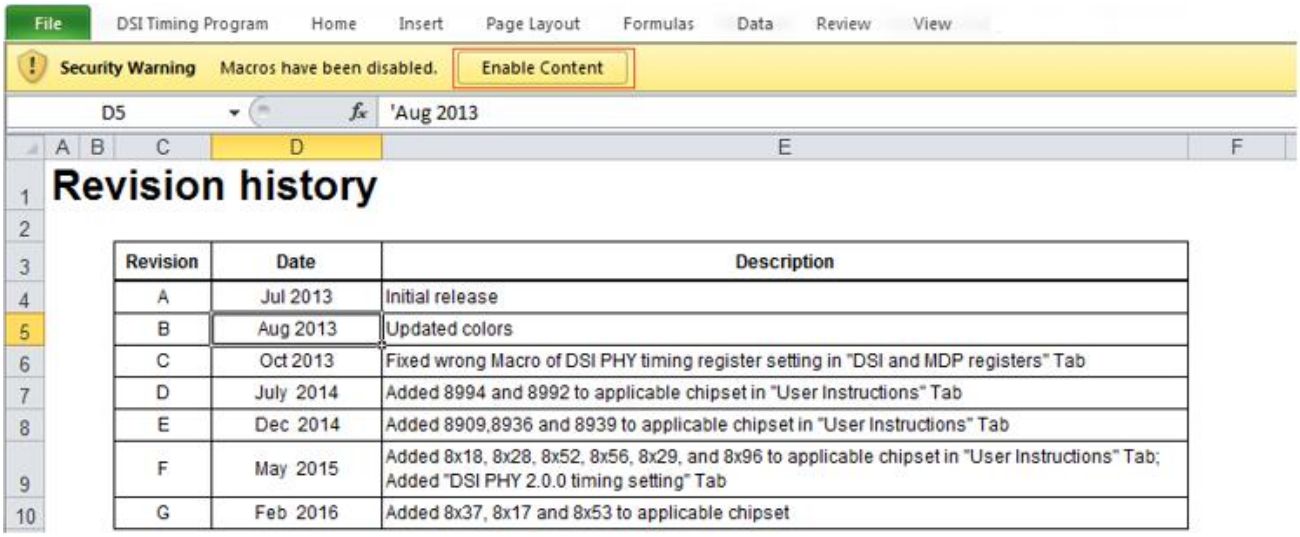
The panel requires the PHY value setup for "bitclk" in the DSI PHY register. The *80-NH713-1_U_DSI_Timing_Parameters_User_Interactive_Spreadsheet.xlsm* in *80-NH713-1_DSI.zip* (the zip file is available in tools directory) can be used to calculate the timing values automatically.

NOTE

Please use Microsoft Excel (Microsoft Excel 2016 is recommended) to open this file. Other tools, such as WPS, are not recommended.

To auto-calculate these values, please take the following steps:

1. Open the 80-NH713-1_U_DSI_Timing_Parameters_User_Interactive_Spreadsheet.xlsm and click **Enable Content**.

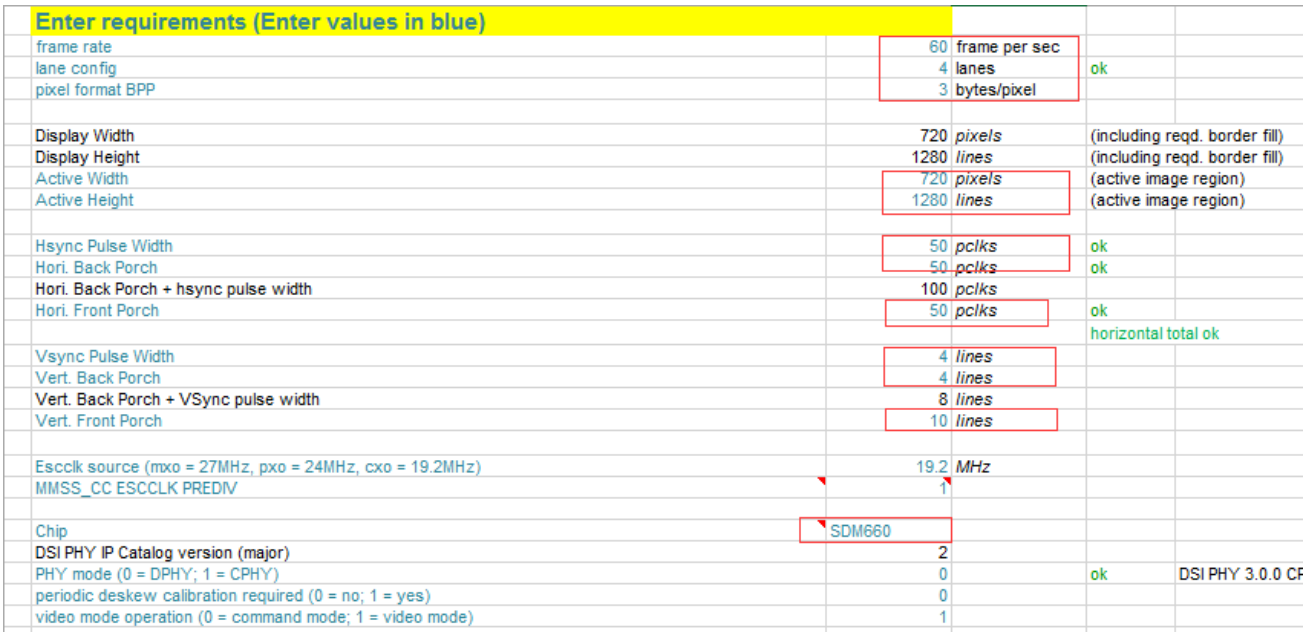


Revision history

Revision	Date	Description
A	Jul 2013	Initial release
B	Aug 2013	Updated colors
C	Oct 2013	Fixed wrong Macro of DSI PHY timing register setting in "DSI and MDP registers" Tab
D	July 2014	Added 8994 and 8992 to applicable chipset in "User Instructions" Tab
E	Dec 2014	Added 8909,8936 and 8939 to applicable chipset in "User Instructions" Tab
F	May 2015	Added 8x18, 8x28, 8x52, 8x56, 8x29, and 8x96 to applicable chipset in "User Instructions" Tab; Added "DSI PHY 2.0.0 timing setting" Tab
G	Feb 2016	Added 8x37, 8x17 and 8x53 to applicable chipset

Figure 1: Enable Content

2. Open the **DSI and MDP Registers** sheet. Input *frame rate/lane numbers/panel resolution/porch/ chip* value to the area framed in red line in the example shown below:



Enter requirements (Enter values in blue)				
frame rate	60	frame per sec		
lane config	4	lanes	ok	
pixel format BPP	3	bytes/pixel		
Display Width	720	*pixels*	(including reqd. border fill)	
Display Height	1280	*lines*	(including reqd. border fill)	
Active Width	720	*pixels*	(active image region)	
Active Height	1280	*lines*	(active image region)	
Hsync Pulse Width	50	*pclks*	ok	
Hori. Back Porch	50	*pclks*	ok	
Hori. Back Porch + hsync pulse width	100	*pclks*		
Hori. Front Porch	50	*pclks*	ok	
			horizontal total ok	
Vsync Pulse Width	4	*lines*		
Vert. Back Porch	4	*lines*		
Vert. Back Porch + VSync pulse width	8	*lines*		
Vert. Front Porch	10	*lines*		
Escclk source (mxo = 27MHz, pxo = 24MHz, cxo = 19.2MHz)	19.2	*MHz*		
MMSS_CC ESCCLK PREDIV	1			
Chip	SDM660			
DSI PHY IP Catalog version (major)	2			
PHY mode (0 = DPHY; 1 = CPHY)	0		ok	DSI PHY 3.0.0 CF
periodic deskew calibration required (0 = no; 1 = yes)	0			
video mode operation (0 = command mode; 1 = video mode)	1			

Figure 2: DSI and MDP Registers Sheet

NOTE

If the spreadsheet requires to change the porches to be multiple of 4 or make it even, please change it accordingly and also update the panel porch node. Users can refer to the user instructions in the Excel sheet.

3. Open the **DSI PHY Timing Setting** sheet to see the calculated DSI-related clock rate in the blue fields. Press **CTRL+J**, a value of **INVALID** will appear in the **Check for T_CLK_ZERO** field. Then press **CTRL+K** to recalculate **T_CLK_ZERO** to **VALID**, as shown below.

1	**1. PHY Timing parameters calculated from bitclk calculated in "dsi and mdp registers" and escclk source set in "dsi and mdp**							
2	**(User may overwrite the values in blue)**							
3	**Full Rate Bitclk**	1141.00	Mbps					
4	**escclk**	19.2	MHz				Check for T_CLK_ZERO	INVALID
5	**UI**	0.876424189	ns					
6	**Tlpx**	52.08333333	ns					
7	**Treot**	20	ns					
8		MIPI PHY v1.1 requirement		Recommended register settings (dec)			program value	theoretical
9		min (ns)	max (ns)	min	max		(hardwired to PHY inputs)	value (ns)
10	T_CLK_PREPARE	38	95	42	107	48	48	43.82120947
11	T_CLK_ZERO	256.1787905		291	511	320	INVALID	#VALUE!
12	T_CLK_TRAIL	60	95.51709027	67	107	70	70	63.10254163
13	T_HS_PREPARE	43.50569676	90.25854514	48	101	54	54	50.83260298
14	T_HS_ZERO	102.9316389		116	255	130	130	115.687993
15	T_HS_TRAIL	63.50569676	95.51709027	71	107	74	74	66.60823839
16	T_HS_RQST					59	59	52.58545136
17	T_HS_EXIT	100		113	255	128	128	113.9351446
18	T_TA_GO	208.3333333	208.3333333			208.3333333	3	208.3333333
19	T_TA_SURE	52.08333333	104.1666667			52.08333333	0	104.1666667
20	T_TA_GET	260.4166667	260.4166667			260.4166667	4	260.4166667
21	TEOT of data lane		115.5170903					76.60823839
22	TEOT of clock lane		115.5170903					73.10254163
23	T_CLK_POST	105.5740578		-6	63	1	1	148.9921122
24	T_CLK_PRE	7.011393514		#VALUE!	63	#VALUE!	#VALUE!	#VALUE!
25	overhead in data transmission							#VALUE!

Figure 3: INVALID in DSI PHY Timing Setting Sheet

1	**1. PHY Timing parameters calculated from bitclk calculated in "dsi and mdp registers" and escclk source set in "dsi and mdp registers"**							
2	**(User may overwrite the values in blue)**							
3	**Full Rate Bitclk**	849.00	Mbps					
4	**escclk**	19.2	MHz				Check for T_CLK_ZERO	VALID
5	**UI**	1.177856302	ns					
6	**Tlpx**	52.08333333	ns					
7	**Treot**	20	ns					
8		MIPI PHY v1.1 requirement		Recommended register settings (dec)			program value	actual value (ns
9		min (ns)	max (ns)	min	max		(hardwired to PHY inputs)	
10	T_CLK_PREPARE	38	95	31	79	53	53	63.60424028
11	T_CLK_ZERO	236.3957597		199	255	209	209	247.3498233
12	T_CLK_TRAIL	60	99.13427562	49	83	51	51	61.24852768
13	T_HS_PREPARE	44.71142521	92.06713781	36	77	55	55	65.95995289
14	T_HS_ZERO	90.81861013		76	255	83	83	98.93992933
15	T_HS_TRAIL	64.71142521	99.13427562	53	83	56	56	68.31566549
16	T_HS_RQST					42	42	51.82567727
17	T_HS_EXIT	100		83	255	92	92	110.7184923
18	T_TA_GO	208.3333333	208.3333333			208.3333333	3	208.3333333
19	T_TA_SURE	52.08333333	104.1666667			52.08333333	0	104.1666667
20	T_TA_GET	260.4166667	260.4166667			260.4166667	4	260.4166667
21	TEOT of data lane		119.1342756					78.31566549
22	TEOT of clock lane		119.1342756					71.24852768
23	T_CLK_POST	121.2485277		-3	63	4	4	186.1012956
24	T_CLK_PRE	9.422850412		39	63	42	42	42.14517079
25	overhead in data transmission							1057.714959
26								

clock related information

T_CLK_ZERO:
This is a SW workaround for Aragorn V1:
If G4 cell states "VALID", then use all programming values as listed.

If G4 states INVALID, press **CTRL + K** to auto-calculate new Tclk_zero program value.

Press **CTRL + J** to return to default equation.

Figure 4: VALID in DSI PHY Timing Setting Sheet

The spreadsheet will show the PHY value setup for “bitclk” which the panel requires in the DSI PHY register.

20	T_TA_GET	260.4166667	260.4166667			260.4166667	4	260.4166667
21	TEOT of data lane		134.2682927					83.17073171
22	TEOT of clock lane		134.2682927					78.29268293
23	T_CLK_POST	186.8292683		-3	63	4	4	307.3170732
24	T_CLK_PRE	19.51219512		21	63	26	26	128.4044715
25	overhead in data transmission							1424.390244
26								
27	**2. DSI PHY registers**							
28	PHY Registers	value in hex						
29	DSIPHY_TIMING_CTRL_0	7B						
30	DSIPHY_TIMING_CTRL_1	1A						
31	DSIPHY_TIMING_CTRL_2	10						
32	DSIPHY_TIMING_CTRL_3	0						
33	DSIPHY_TIMING_CTRL_4	3C						
34	DSIPHY_TIMING_CTRL_5	42						
35	DSIPHY_TIMING_CTRL_6	14						
36	DSIPHY_TIMING_CTRL_7	1C						
37	DSIPHY_TIMING_CTRL_8	15						
38	DSIPHY_TIMING_CTRL_9	3						
39	DSIPHY_TIMING_CTRL_10	4						
40								
41	**3. DSI Registers (address)**							
42	DSI_CLKOUT_TIMING_CTRL	41A						
43	DSI_TEST_PATTERN_GEN_VIDEO_ENABLE	0						

Figure 5: PHY Value Setting in the Spreadsheet

4. Update the panel XML file **<PanelTimings>** with the values listed above that obtained from the Excel worksheet.

The following is an example. The following values are copied from ***Figure 5***.

```
<PanelTimings>"0x7B, 0x1A, 0x10, 0x00, 0x3C, 0x42, 0x14, 0x1C, 0x15, 0x03,
0x04,0x00"</PanelTimings>
```

5. Copy the program value for **T_CLK_POST** and **T_CLK_PRE** fields obtained from the Excel worksheet into the panel XML. The values in the Excel worksheet are in decimal. Make sure that they are converted to HEX before updating the two elements.

```
<TClkPost>0x4</TClkPost>
<TClkPre>0x1A</TClkPre>
```

6. For SC66, DSI PHY 2.0.0 timing configuration needs to be added, and it can be found in *kernel/msm-4.4/arch/arm/boot/dts/qcom/sdm660-mdss-panels.dtsi*, as shown below:

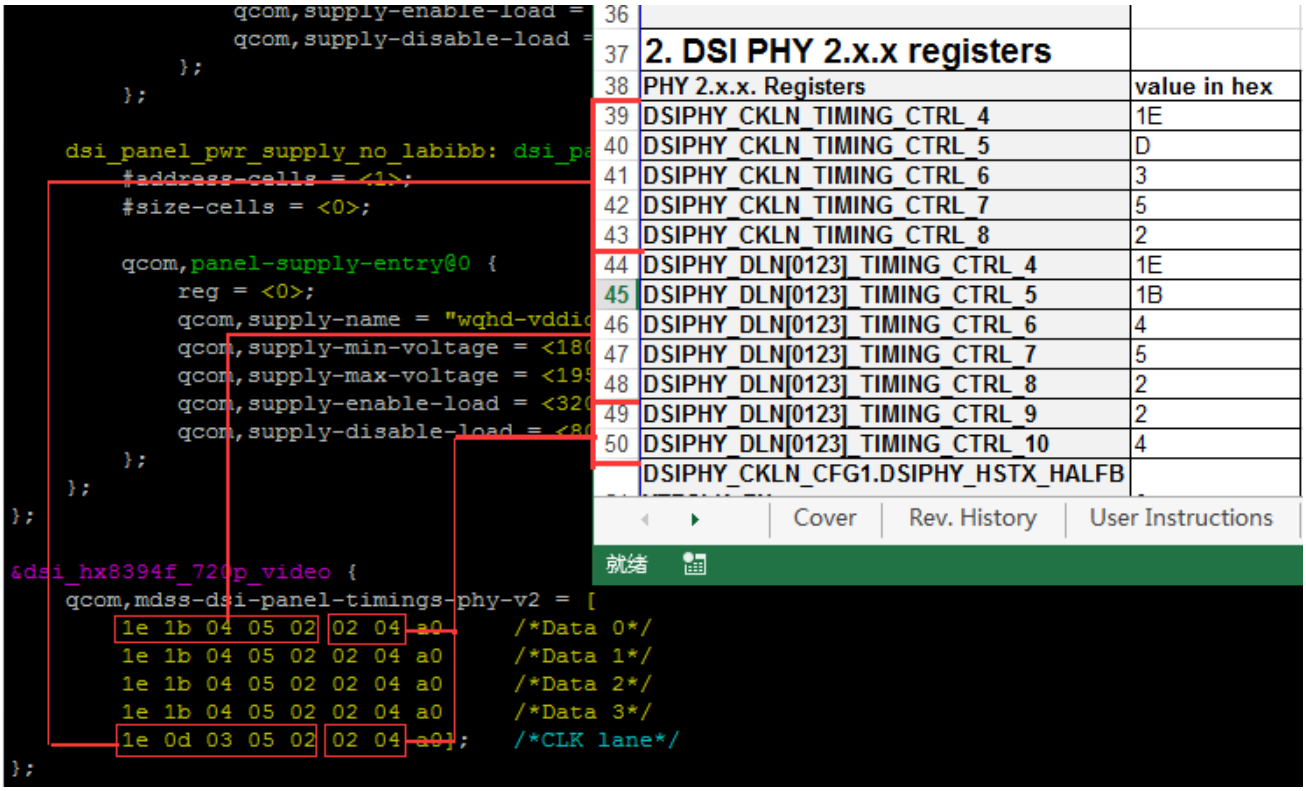


Figure 6: DSI PHY 2.0.0 Timing Configuration for SC66 Module

2.7. Command Mode Panel

All TE-related entries listed in the following table are only used in Android kernel.

These parameters are only used in command mode panel. If the LCD is a video mode panel, these parameters can be ignored.

Table 10: TE-related Entries

Entry	Description	Value
TECheckEnable	It enables/disables the TE to check hardware block within MDP.	0=Disabled 1=Enabled
TEPinSelect	It controls TE to check hardware block through external GPIO pin or an embedded TE signal.	0=through an embedded TE signal 1=through GPIO pin
TEUsingTEPin	It controls TE to check hardware block through software vertical synchronization or hardware vertical synchronization.	0=Software vertical synchronization 1=Hardware vertical synchronization
TEvSyncRdPtrIrqLine	This integer configures the scan line number that the DSI pixel transfer will start on. This should be left at the default value of 0. Adjusting this number to a higher value will result in delay in the start of the pixel transfer.	
TEvSyncContinueLines	This integer represents the difference in the number of lines between estimated read pointer and write pointer to allow the updating of all the lines except the first line of the frame. This threshold is maintained only when Tear Check block is enabled.	
TEDCSCommand	This entry inserts the DCS command.	

For example

```
<!--- command mode panel -->
<TECheckEnable>1</TECheckEnable>
<TEPinSelect>1</TEPinSelect>
<TEUsingTEPin>1</TEUsingTEPin>
<TEvSyncRdPtrIrqLine>0x2c</TEvSyncRdPtrIrqLine>
<TEvSyncContinueLines>0x3c</TEvSyncContinueLines>
<TEDCSCommand>1</TEDCSCommand>
```

2.8. Backlight Configuration

This chapter describes the various backlight configuration entries.

Table 11: Backlight Configuration

Entry	Description	Value
BLMinLevel	Minimum value of backlight.	1
BLMaxLevel	Maximum value of backlight.	4095
BLPMICControlType	PMIC controller for current backlight.	0=PWM GPIO 1=WLED 2=DCS COMMANDS (for OLED panel backlight controller) 3=LPG

For example:

```
<!-- Backlight -->
<BLInterfaceType>1</BLInterfaceType>
<BLMinLevel>1</BLMinLevel>
<BLMaxLevel>4095</BLMaxLevel>
<BLStep>100</BLStep>
<BLPMICModel>"PMIC 8941"</BLPMICModel>
<BLPMICControlType>0</BLPMICControlType>
```

3 Configure Kernel and UEFI

NOTE

Panel parameters are configured in both UEFI and kernel. After startup, configuration parameters in UEFI will be used to drive the panel before pressing the power key. After system sleep and then wakeup, configuration parameters in kernel will be used to drive the panel.

3.1. Configure Kernel

After the procedure in ***Chapter 2.1*** is completed, the file *dsi-panel-hx8394f-720p-video.dtsi* will be generated, then copy it to the following directory *kernel/msm-4.4/arch/arm64/boot/dts/qcom/*. And then configure the kernel to add a new panel according to the following steps.

1. Include .dtsi files

Include the .dtsi file to the *kernel/msm-4.4/arch/arm64/boot/dts/qcom/sdm660-mdss-panels.dtsi* file.

```
#include "dsi-panel-hx8394d-wxga-video.dtsi"
#include "dsi-panel-inxnt51021-1200p-video.dtsi"
#include "dsi-panel-ili9881c-720p-video.dtsi"
#include "dsi-panel-ili9881c-720p-dsi1-video.dtsi"
#include "dsi-panel-hx8394f-720p-video.dtsi"
#include "dsi-panel-hx8394f-720p-dsi1-video.dtsi"
```

2. Modify .dtsi files

Add DSI PHY 2.0.0 timing configuration to the following directory:
kernel/msm-4.4/arch/arm64/boot/dts/qcom/ sdm660-mdss-panels.dtsi.

```
&dsi_hx8394f_720p_video {
    qcom,mdss-dsi-panel-timings-phy-v2 = [
        1e 1b 04 05 02 03 04 a0     /*Data 0*/
        1e 1b 04 05 02 03 04 a0     /*Data 1*/
        1e 1b 04 05 02 03 04 a0     /*Data 2*/
        1e 1b 04 05 02 03 04 a0     /*Data 3*/
        1e 0d 03 05 02 03 04 a0];   /*CLK lane*/
};
```

The following should be modified as well in *kernel/msm-4.4/arch/arm/boot/dts/qcom/sdm660-mtp.dtsi*.

```
&mdss_dsi0 {
    qcom,dsi-pref-prim-pan = <&dsi_hx8394f_720p_video>;
    pinctrl-names = "mdss_default", "mdss_sleep";
    pinctrl-0 = <&mdss_dsi_active &mdss_te_active>;
    pinctrl-1 = <&mdss_dsi_suspend &mdss_te_suspend>;
    qcom,platform-reset-gpio = <&tlmm 53 0>;
    qcom,platform-te-gpio = <&tlmm 59 0>;
};
```

3. Configure the backlight

Configure the backlight in the *kernel/msm-4.4/arch/arm64/boot/dts/qcom/sdm660-mtp.dtsi* directory.

```
&dsi_hx8394f_720p_video {
    qcom,mdss-dsi-bl-pmic-control-type = "bl_ctrl_pwm";
    qcom,mdss-dsi-bl-pmic-pwm-frequency = <100>; /* in microseconds */
    qcom,mdss-dsi-bl-pmic-bank-select = <0>;
    qcom,mdss-dsi-bl-pwm-pmi;
    pwms = <&pm660l_pwm_4 0 0>;
    qcom,panel-supply-entries = <&dsi_panel_pwr_supply>;
};
```

To configure backlight, the backlight type should be configured.

qcom,mdss-dsi-bl-pmic-control-type: a string that specifies the implementation of backlight control for this panel.

If the following values are configured in the red-framed area of the above figure, then:
"bl_ctrl_pwm" indicates backlight controlled by PWM
"bl_ctrl_wled" indicates backlight controlled by WLED
"bl_ctrl_dcs" indicates backlight controlled by DCS commands (for OLED panel backlight controller).
Others: Unknown backlight control.

- For the PWM default backlight control, select the “control-type”, “pwm-frequency” and “pwms” shown below:

```
&dsi_hx8394f_720p_video {
        qcom,mdss-dsi-bl-pmic-control-type = "bl_ctrl_pwm";
        qcom,mdss-dsi-bl-pmic-pwm-frequency = <100>;/* in microseconds */
        qcom,mdss-dsi-bl-pmic-bank-select = <0>;
        qcom,mdss-dsi-bl-pwm-pmi;
        pwms = <&pm660l_pwm_4 0 0>;
        qcom,panel-supply-entries = <&dsi_panel_pwr_supply>;
};
```

- For the WLED backlight control, select the “control-type” shown as below.

The path is *kernel/msm-4.4/arch/arm64/boot/dts/qcom/sdm660-mtp.dtsi*

```
&dsi_dual_nt35597_truly_video {
            qcom,mdss-dsi-bl-pmic-control-type = "bl_ctrl_wled";
            qcom,mdss-dsi-bl-min-level = <1>;
            qcom,mdss-dsi-bl-max-level = <4095>;
            qcom,mdss-dsi-mode-sel-gpio-state = "dual_port";
            qcom,panel-supply-entries = <&dsi_panel_pwr_supply>;
    };
```

- Control the backlight by sending the DCS commands at any point.

The path is *./kernel/msm-4.4/arch/arm/boot/dts/qcom/dsi-panel-rm67195-amoled-fhd-cmd.dtsi*

```
qcom,mdss-dsi-bl-min-level = <1>;
qcom,mdss-dsi-bl-max-level = <255>;
qcom,mdss-dsi-bl-pmic-control-type = "bl_ctrl_dcs";
```

Use the following code to send the backlight command.
Path: *./kernel/msm-4.4/drivers/video/fbdev/msm/mdss_dsi_panel.c*

```
static char led_pwm1[2] = {0x51, 0x0};    /* DTYPE_DCS_WRITE1 */
static struct dsi_cmd_desc backlight_cmd = {
      {DTYPE_DCS_WRITE1, 1, 0, 0, 1, sizeof(led_pwm1)},
      led_pwm1
};
```

4. Change cmdline information

According to the panel .dtsi file to get the cmdline information.
Path: *kernel/msm-4.4/arch/arm/boot/dts/qcom/dsi-panel-hx8394f-720p-video.dtsi*

```
&mdss_mdp {
    dsi_hx8394f_720p_video: qcom,mdss_dsi_hx8394f_720p_video {
        qcom,mdss-dsi-panel-name = "hx8394f 720p video mode dsi panel";
        qcom,mdss-dsi-panel-controller = <&mdss_dsi0>;
        qcom,mdss-dsi-panel-type = "dsi_video_mode";
        qcom,mdss-dsi-panel-destination = "display_1";
```

Add the following code to change the default cmdline information.
Path: *kernel/msm-4.4/drivers/video/fbdev/msm/mdss_dsi.c.*

```
+++ b/kernel/msm-4.4/drivers/video/fbdev/msm/mdss_dsi.c
@@ -3184,8 +3184,10 @@ static struct device_node *mdss_dsi_find_panel_of_node(
        struct device_node *dsi_pan_node = NULL, *mdss_node = NULL;
        struct mdss_dsi_ctrl_pdata *ctrl_pdata = platform_get_drvdata(pdev);
        struct mdss_panel_info *pinfo = &(ctrl_pdata->panel_data.panel_info);
+       char panel_cfg_cmdline[] = "0:qcom,mdss_dsi_hx8394f_720p_video:config0:1:none:cfg:single_dsi";

        len = strlen(panel_cfg);
+       strcpy(panel_cfg, panel_cfg_cmdline);
        ctrl_pdata->panel_data.dsc_cfg_np_name[0] = '\0';
        if (!len) {
                /* no panel cfg chg, parse dt */
```

3.2. Update UEFI

The bootloader of SC66 was replaced by UEFI and the source code of UEFI has not been publiclly unavailable. Therefore, to configure the UEFI, users should take the following steps:

1. Bring up their own LCD in kernel.
2. Send the LCD parameters they obtained from ***Step 1*** to Quectel.
3. Remove the modified cmdline code if the LCD is brought up in both UEFI and kernel.

After this, Quectel will update the bin file *xbl.elf* for users.

After being updated by Quectel, users are able to update the xbl.elf file with Fastboot by the following commands to verify whether the LCD in UEFI has been brought up. If not, please contact Quectel.

```
adb reboot bootloader
fastboot flash xbl xbl.elf
fastboot reboot
```

4 Appendix

Table 12: Terms and Abbreviations

Abbreviation	Description
DCS	Display Command Set
DSI	Display Serial Interface
GCDB	Global Component Database
GPIO	General Purpose Input Output
LCD	Liquid Crystal Display
LK	Little Kernel
LPG	Light Pulse Generator
MDP	Mobile Display Processor
PMIC	Power Management IC
PWM	Pulse Width Modulation
TE	Tearing Effect
WLED	White Light Emitting Diode
UEFI	Unified Extensible Firmware Interface