

BG95xA&EG915U&EG91xQ Series

Compatible Design

LTE Standard & LPWA Module Series

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About the Document

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1 Introduction

Quectel LPWA BG95xA-GL are compatible with LTE Standard EG915U series and EG91xQ family. This document outlines the compatible design among these modules.

NOTE

Blue text indicates the differences among BG95xA-GL, EG915U series and EG91xQ family, unless otherwise specified.

1.1. Special Mark

Table 1: Special Mark

Mark	Definition
*	Unless otherwise specified, an asterisk (*) after a function, feature, interface, pin name, command, argument, and so on indicates that it is under development and currently not supported; and the asterisk (*) after a model indicates that the model sample is currently unavailable.

1.2. Applicable Modules

Table 2: Applicable Modules

Product Line	Module Family	Module Series	Model
			BG950A-GL
LPWA	BG95xA	-	BG951A-GL
			BG955A-GL

			EG915U-CN
	-	EG915U	EG915U-LA
			EG915U-EU
LTE Standard			EG915Q-NA
	EG91xQ	EG915Q	EG915Q-AF
			EG915Q-JP
		-	EG916Q-GL

2 General Description

2.1. Product Description

BG95xA-GL is an embedded IoT wireless communication module. It supports data connectivity on LTE HD-FDD network, and features GNSS functionality to meet your specific application demands.

EG915U series module is an LTE and GSM wireless communication module, which provides data connectivity on LTE-FDD, LTE-TDD, and GPRS networks. It also provides voice functionality, Bluetooth and Wi-Fi Scan to meet your specific application demands.

EG91xQ family is an LTE Standard wireless communication module. It supports data connectivity on LTE network, Wi-Fi scan and GNSS to meet your specific application demands.

Table 3: Supported Frequency Bands and Functions of the Modules

Frequency Bands and Functions	BG95xA-GL	EG915U Series	EG91xQ Family
LTE-FDD	LTE-HD-FDD	√	√
LTE-TDD	-	EG915U-CN: √ EG915U-EU/LA: -	EG915Q series: - EG916Q-GL: √
GSM/GPRS	BG950A-GL: - BG951A-GL: - BG955A-GL: GPRS	√	-
Voice Functionality	-	√	-
Wi-Fi Scan	-	○	√
Bluetooth	-	○	-
GNSS	√	-	○

NOTE

1. “√” means supported.

2. “-” means not supported.
3. “o” means optional.
4. **BG95xA-GL**: The baseband chip of BG950A-GL and BG955A-GL integrates the GNSS function, whereas the internal baseband chip and GNSS chip are separated on BG951A-GL. Therefore, BG951A-GL supports concurrent operation of LTE and GNSS, whereas BG950A-GL and BG955A-GL do not. It is important to note that GNSS cannot operate independently in Power Saving Mode (PSM) and cannot be woken up. For details, please contact Quectel Technical Support.
5. **EG915U series**: The module supports Bluetooth and Wi-Fi Scan functions. Due to the shared antenna interface, the two functions cannot be used simultaneously. Bluetooth and Wi-Fi Scan functions are optional, and please contact Quectel Technical Support for details.
6. **EG91xQ family**: Wi-Fi Scan function shares the same antenna interface with the main antenna. These two antennas should use TDM (Time Division Multiplexing) and cannot be used simultaneously. Wi-Fi Scan only supports receiving and does not support transmitting.

2.1.1. General Information

Table 4: General Information

Module	Appearance	Packaging	Dimensions (mm)	Description
BG95xA-GL		102 LGA pins	23.6 × 19.9 × 2.2	LPWA module
EG915U series		126 LGA pins	23.6 × 19.9 × 2.4	LTE Standard module

EG915Q series



126 LGA pins

23.6 × 19.9 × 2.4

LTE Standard
module

EG916Q-GL



126 LGA pins

26.5 × 22.5 × 2.4

LTE Standard
module

2.2. Feature Overview

Table 5: Feature Overview

Feature	BG95xA-GL	EG915U Series	EG91xQ Family
Power Supply	BG950A-GL/BG951A-GL: <ul style="list-style-type: none"> Supply voltage: 2.2–4.35 V Typical supply voltage: 3.3 V BG955A-GL: <ul style="list-style-type: none"> Supply voltage: 3.3–4.3 V Typical supply voltage: 3.8 V 	<ul style="list-style-type: none"> Supply voltage: 3.3–4.3 V Typical supply voltage: 3.8 V 	<ul style="list-style-type: none"> Supply voltage: 3.3–4.3 V Typical supply voltage: 3.8 V
Peak Current	BG950A-GL/BG951A-GL: VBAT_BB/RF: 0.8 A BG955A-GL: VBAT_BB/RF: 2.3 A	VBAT_BB: 1.0 A VBAT_RF: 2.5 A	VBAT_BB: 0.3 A VBAT_RF: 1.2 A
Turn-off Current	Turn-off @ USB/UART disconnected: 1.5 μA	32.0 μA @ EG915U-CN/EU 36.8 μA @ EG915U-LA	0.4 μA @ EG915Q-NA 0.5 μA @ EG915Q-AF/JP, EG916Q-GL
Sleep Current	AT+CFUN=0 @ Sleep mode: 39 μA @ BG950A-GL 42 μA @ BG951A-GL, BG955A-GL	AT+CFUN=0 (USB disconnected) 1.0 mA @ EG915U-CN 1.1 mA @ EG915U-EU 0.94 mA @ EG915U-LA	AT+CFUN=0 (USB disconnected): 54 μA @ EG915Q-NA, EG916Q-GL 61 μA @ EG915Q-AF 59 μA @ EG915Q-JP
Temperature Range	<ul style="list-style-type: none"> Operating temperature range ¹: -35 to +75 °C Extended temperature range ²: -40 to +85 °C Storage temperature range: -40 to +90 °C 	<ul style="list-style-type: none"> Operating temperature range ¹: -35 to +75 °C Extended temperature range ²: -40 to +85 °C Storage temperature range: -40 to +90 °C 	<ul style="list-style-type: none"> Operating temperature range ¹: -35 to +75 °C Extended temperature range ²: -40 to +85 °C Storage temperature range: -40 to +90 °C
(U)SIM Interfaces	1.8 V external (U)SIM/eSIM card only	<ul style="list-style-type: none"> 1.8/3.0 V (U)SIM Supports Dual SIM Single Standby by default ³ 	<ul style="list-style-type: none"> USIM1: 1.8/3.0 V ⁴ USIM2: 1.8 V ⁵ Only support Dual SIM Single Standby
USB Interface	<ul style="list-style-type: none"> Compliant with USB 2.0 specification (slave only). Data transmission rate: up to 12 Mbps. Supports full-speed mode only Used for AT command communication, data transmission, software debugging and firmware upgrade* Supports USB serial drivers for Windows 8.1/10/11, Linux 2.6–6.7 	<ul style="list-style-type: none"> Compliant with USB 2.0 specification (slave only). Data transmission rate: up to 480 Mbps. Supports high-speed and full-speed modes. Used for AT command communication, data transmission, software debugging and firmware upgrade Supports USB serial drivers for Windows 8.1/10/11, Linux 2.6–6.7, Android 4.x–14.x. 	<ul style="list-style-type: none"> Compliant with USB 2.0 specification (slave only). Data transmission rate: up to 480 Mbps. Supports high-speed and full-speed modes. Used for AT command communication, data transmission, GNSS NMEA sentence output (All-in-one mode only), software debugging, firmware upgrade and the output of partial logs. Supports USB serial drivers for Windows 8.1/10/11, Linux 2.6–6.7, Android 4.x–14.x.

¹ Within the operating temperature range, the module meets 3GPP specifications.

² Within the extended temperature range, the module retains the ability to establish and maintain functions such as voice (only for EG915U series), SMS, data transmission and emergency call (only for EG915U series), without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as P_{out}, may exceed the specified 3GPP tolerances. When the temperature returns to the operating temperature range, the module meets 3GPP specifications again.

³ Please contact Quectel Technical Support if Dual SIM Dual Standby is required.

⁴ When USIM1 and USIM2 are used at the same time, the power domain of USIM interfaces should be 1.8 V. Otherwise, USIM2 interface will be damaged.

⁵ USIM2 and camera SPI* cannot be used at the same time.

UART Interfaces	<p>Main UART:</p> <ul style="list-style-type: none"> ● Used for AT command communication and data transmission ● Baud rate: up to 3000000 bps; 115200 bps by default. ● Default frame format: 8N1 (8 data bits, no parity, 1 stop bit). ● RTS and CTS hardware flow control. <p>Debug UART:</p> <ul style="list-style-type: none"> ● Used for RF calibration and SFP log output ● Baud rate: 921600 bps by default ● Default frame format: 8N1 (8 data bits, no parity, 1 stop bit) ● RTS and CTS hardware flow control <p>GNSS UART (Only BG951A-GL):</p> <ul style="list-style-type: none"> ● Used for GNSS data and GNSS NMEA sentence output, and GNSS firmware upgrade ● Baud rate: 115200 bps by default <p>CLI UART ⁶:</p> <ul style="list-style-type: none"> ● Used for firmware upgrade, software debugging, CLI log output, GNSS data and NMEA sentence output ● Baud rate: 115200 bps by default ● Default frame format: 8N1 (8 data bits, no parity, 1 stop bit) ● RTS and CTS hardware flow control 	<p>Main UART:</p> <ul style="list-style-type: none"> ● Used for AT command communication and data transmission ● Baud rates: up to 921600 bps; 115200 bps by default ● RTS and CTS hardware flow control <p>Debug UART:</p> <ul style="list-style-type: none"> ● Used for log output ● Baud rate: 921600 bps by default ● Cannot be used as a general-purpose UART <p>Auxiliary UART:</p> <ul style="list-style-type: none"> ● The baud rate is the same as that of the main UART 	<p>Main UART:</p> <ul style="list-style-type: none"> ● Used for AT command communication and data transmission ● Baud rates: up to 921600 bps; 115200 bps by default. ● RTS and CTS hardware flow control. <p>Debug UART:</p> <ul style="list-style-type: none"> ● Used for partial log output. ● Baud rate: 115200 bps, 3 Mbps (by default) <p>GNSS UART:</p> <ul style="list-style-type: none"> ● Used for outputting GNSS data or GNSS NMEA sentence output ● Baud rate: 921600 bps <p>GNSS debug UART:</p> <ul style="list-style-type: none"> ● Used for outputting GNSS system logs ● Baud rate: 3 Mbps
ADC	<ul style="list-style-type: none"> ● Two ADC interfaces ● Input voltage range: 0–1.8 V 	<ul style="list-style-type: none"> ● Two ADC interfaces ● Input voltage range: 0–VBAT 	<ul style="list-style-type: none"> ● Two ADC interfaces ● Input voltage range: 0–1.2 V
GRFC	Two GRFC interfaces	Two GRFC interfaces	Two GRFC interfaces
GPIO	Nine GPIO interfaces	-	-
PCM Interface	-	One PCM interface	One PCM interface*
I2C Interface	-	One I2C interface	One I2C interface*
SPI	-	One SPI interface*	One camera SPI interface*
Antenna interfaces	<ul style="list-style-type: none"> ● Main antenna ● GNSS antenna 	<ul style="list-style-type: none"> ● Main antenna ● Bluetooth/Wi-Fi Scan antenna 	<ul style="list-style-type: none"> ● Main/Wi-Fi Scan antenna ● GNSS antenna
Firmware Upgrade	<ul style="list-style-type: none"> ● CLI UART interface ⁶ ● USB 2.0 interface* ● DFOTA 	<ul style="list-style-type: none"> ● USB 2.0 interface ● DFOTA 	<ul style="list-style-type: none"> ● USB 2.0 interface (Only in download mode, the module supports firmware upgrade over USB 2.0 interface) ● DFOTA

⁶ BG951A-GL only supports one CLI UART interface, while BG950A-GL and BG955A-GL support two CLI UART interfaces, more precisely, pin 27 (CLI_TXD1) and pin 28 (CLI_RXD1) are connected to pin 95 (CLI_TXD2) and pin 94 (CLI_RXD2) respectively inside the module.

3 Pin Definition

3.1. Pin Assignment

BG95xA-GL & EG915U Series & EG91xQ Family

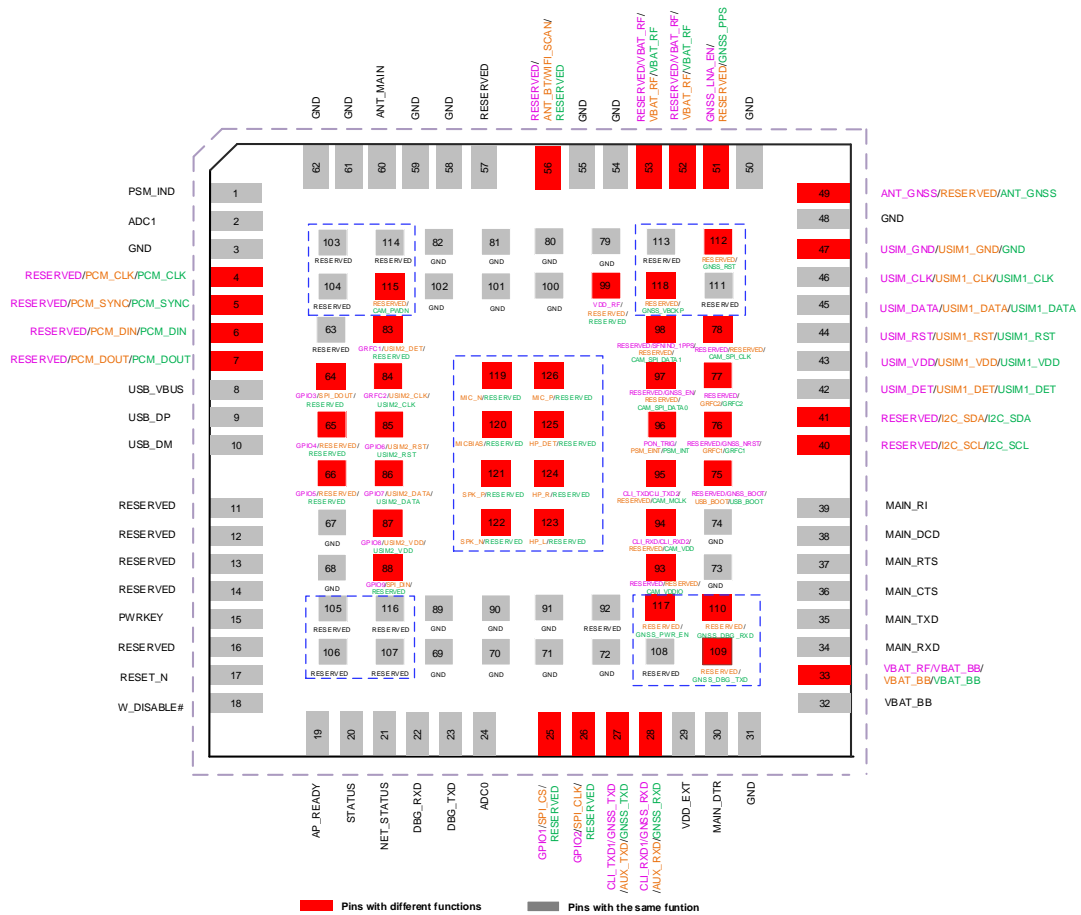


Figure 1: Pin Assignment of BG95xA-GL & EG915U & EG91xQ Family (Top View)

NOTE

1. Pins within the blue dashed box are only supported by the EG915U series and EG91xQ family. There are no pins for the BG95xA-GL in this area.

2. The dimensions of the EG916Q-GL are slightly larger than those of other modules. For the purpose of differentiation, the outer **gray** dashed border represents the dimensions of the EG916Q-GL, and the inner **black** solid border represents the dimensions of the BG95xA-GL, EG915U and EG915Q series.
3. Pins 27, 28, 33, 52, 53, 75, 76, 94, 95, 97 and 98 have different functions on BG950A-GL, BG951A-GL and BG955A-GL. For more details, see **document [1]**.
4. Keep all RESERVED and unused pins unconnected.
5. Connect GND pins to the ground in the design.
6. **EG915U Series:**
When using pins 18, 19, 30, 38, and 39 (W_DISABLE#, AP_READY, MAIN_DTR, MAIN_DCD and MAIN_RI), please note that these pins will have a period of variable level state (not controllable by software) after the module is turned on: at high level (3.0 V) for 2 s and then at low level (0 V) for 1.2 s before they can be configured as 1.8 V input or output. Evaluate whether the unstable level output state on turn-on meets your application design requirements based on the specific usage scenario and circuit design.
7. **EG91xQ Family:**
 - 1) In sleep mode, pins 34–37 of the main UART interface, pins 22 and 23 of debug UART interface, USB_BOOT (pin 75), pins 4–7 of PCM interface*, pins 40 and 41 of I2C interface*, and pins 78, 93, 95, 97, 98 and 115 of Camera SPI* are powered down. The driving capacity will be lost and the functions of status indication and data transmission are disabled. Pay attention to it when designing circuits.
 - 2) When USIM1 and USIM2 are used at the same time, the power domain of USIM interfaces should be 1.8 V. Otherwise, USIM2 interface will be damaged.

Table 6: I/O Parameter Definition

Type	Description
AI	Analog Input
AIO	Analog Input/Output
DI	Digital Input
DIO	Digital Input/Output
DO	Digital Output
OD	Open Drain
PI	Power Input
PO	Power Output

3.2. Pin Comparison

Table 7: Pin Comparison

Pin No.	BG95xA-GL			EG915U Series			EG91xQ Family			Description
	Pin Name	I/O	Power Domain	Pin Name	I/O	Power Domain	Pin Name	I/O	Power Domain	
1	PSM_IND	DO	1.8 V	PSM_IND*	DO	1.8 V	PSM_IND*	DO	1.8 V	Indicate the module's power saving mode.
2	ADC1	AI	0–1.8 V	ADC1	AI	0–VBAT	ADC1	AI	0–1.2 V	General-purpose ADC interface.
3	GND	-	-	GND	-	-	GND	-	-	Ground.
4	RESERVED	-	-	PCM_CLK	DI	1.8 V	PCM_CLK*	DO	1.8 V	PCM clock.
5	RESERVED	-	-	PCM_SYNC	DI	1.8 V	PCM_SYNC*	DO	1.8 V	PCM data frame sync.
6	RESERVED	-	-	PCM_DIN	DI	1.8 V	PCM_DIN*	DI	1.8 V	PCM data input.
7	RESERVED	-	-	PCM_DOUT	DO	1.8 V	PCM_DOUT*	DO	1.8 V	PCM data output.
8	USB_VBUS	AI	Type: 5.0 V	USB_VBUS	AI	3.5–5.25 V (Type: 5.0 V)	USB_VBUS	AI	3.0–5.25 V (Type: 5.0 V)	USB connection detect.
9	USB_DP	AIO	-	USB_DP	AIO	-	USB_DP	AIO	-	USB differential data (+).
10	USB_DM	AIO	-	USB_DM	AIO	-	USB_DM	AIO	-	USB differential data (-).
11-14	RESERVED	-	-	RESERVED	-	-	RESERVED	-	-	Reserved.
15	PWRKEY ⁷	DI	0.8–2 V	PWRKEY	DI	VBAT power domain.	PWRKEY	DI	1.8 V	Turn on/off the module.
16	RESERVED	-	-	RESERVED	-	-	RESERVED	-	-	Reserved.
17	RESET_N	DI	0.8–2 V	RESET_N	DI	VBAT	RESET_N	DI	1.8 V	Reset the module.
18	W_DISABLE#	DI	1.8 V	W_DISABLE#	DI	1.8 V	W_DISABLE#*	DI	1.8 V	Airplane mode control.
19	AP_READY	DI	1.8 V	AP_READY	DI	1.8 V	AP_READY*	DI	1.8 V	Application processor ready
20	STATUS	DO	1.8 V	STATUS	DO	1.8 V	STATUS	DO	1.8 V	Indicate the module's operation status.
21	NET_STATUS	DO	1.8 V	NET_STATUS	DO	1.8 V	NET_STATUS	DO	1.8 V	Indicate the module's network activity status.
22	DBG_RXD	DI	1.8 V	DBG_RXD	DI	1.8 V	DBG_RXD	DI	1.8 V	Debug UART receive.

⁷ On BG95xA-GL, the minimum high-level output voltage of PWRKEY output is 1.0 V. PWRKEY is internally pulled up to an internal voltage in the baseband chipset, and its output voltage is the internal voltage minus a diode drop in the chipset.

23	DBG_TXD	DO	1.8 V	DBG_TXD	DO	1.8 V	DBG_TXD	DO	1.8 V	Debug UART transmit.
24	ADC0	AI	0–1.8 V	ADC0	AI	0–VBAT	ADC0	AI	0–1.2 V	General-purpose ADC interface.
25	GPIO1	DIO	1.8 V	SPI_CS*	DO	1.8 V	RESERVED	-	-	1. General-purpose input/output. 2. SPI chip select 3. Reserved.
26	GPIO2	DIO	1.8 V	SPI_CLK*	DO	1.8 V	RESERVED	-	-	1. General-purpose input/output. 2. SPI clock. 3. Reserved.
27	CLI_TXD1/ GNSS_TXD	DO	1.8 V	AUX_TXD	DO	1.8 V	GNSS_TXD	DO	1.8 V	1. CLI UART1 transmit/GNSS UART transmit. 2. Auxiliary UART transmit 3. GNSS UART transmit.
28	CLI_RXD1/ GNSS_RXD	DI	1.8 V	AUX_RXD	DI	1.8 V	GNSS_RXD	DI	1.8 V	1. CLI UART1 receive/GNSS UART receive 2. Auxiliary UART receive 3. GNSS UART receive
29	VDD_EXT	PO	1.8 V	VDD_EXT	PO	1.8 V	VDD_EXT	PO	1.8 V	Provide 1.8 V for external circuit.
30	MAIN_DTR	DI	1.8 V	MAIN_DTR	DI	1.8 V	MAIN_DTR	DI	1.8 V	Main UART data terminal ready.
31	GND	-	-	GND	-	-	GND	-	-	Ground.
32	VBAT_BB	PI	BG950A-GL/ BG951A-GL: Voltage range ⁸ : 2.2–4.35 V, Typ. 3.3 V	VBAT_BB	PI	3.3–4.3 V Typ. 3.8 V	VBAT_BB	PI	3.3–4.3 V Typ. 3.8 V	Power supply for the module's BB part.
33	VBAT_RF/ VBAT_BB	PI	BG955A-GL: Voltage range ⁹ : 3.3–4.3 V, Typ. 3.8 V	VBAT_BB	PI	3.3–4.3 V Typ. 3.8 V	VBAT_BB	PI	3.3–4.3 V Typ. 3.8 V	1. Power supply for the module's RF part. 2. Power supply for the module's BB part.
34	MAIN_RXD	DI	1.8 V	MAIN_RXD	DI	1.8 V	MAIN_RXD	DI	1.8 V	Main UART receive.
35	MAIN_TXD	DO	1.8 V	MAIN_TXD	DO	1.8 V	MAIN_TXD	DO	1.8 V	Main UART transmit.
36	MAIN_CTS	DO	1.8 V	MAIN_CTS	DO	1.8 V	MAIN_CTS	DO	1.8 V	Clear to send signal from the module (connect to MCU's CTS)
37	MAIN_RTS	DI	1.8 V	MAIN_RTS	DI	1.8 V	MAIN_RTS	DI	1.8 V	Request to send signal to the module (connect to MCU's RTS)
38	MAIN_DCD	DO	1.8 V	MAIN_DCD	DO	1.8 V	MAIN_DCD	DO	1.8 V	Main UART data carrier detect.
39	MAIN_RI	DO	1.8 V	MAIN_RI	DO	1.8 V	MAIN_RI	DO	1.8 V	Main UART ring indication.
40	RESERVED	-	-	I2C_SCL	OD	-	I2C_SCL*	OD	1.8 V	I2C serial clock

⁸ On BG950A-GL, BG951A-GL and BG953A-GL, every VBAT transition/re-insertion from 0 V, VBAT slew rate < 25 mV/μs. After the module starts up normally, in order to ensure full functionality mode, the minimum power supply voltage should be higher than 2.2 V.

⁹ On BG955A-GL, every VBAT transition/re-insertion from 0 V, VBAT slew rate < 25 mV/μs. After the module starts up normally, in order to ensure full functionality mode, the minimum power supply voltage should be higher than 3.3 V.

41	RESERVED	-	-	I2C_SDA	OD	-	I2C_SDA*	OD	1.8 V	I2C serial data
42	USIM_DET	DI	1.8 V	USIM1_DET	DI	1.8 V	USIM1_DET	DI	1.8 V	(U)SIM card hot-plug detect.
43	USIM_VDD	PO	1.8 V	USIM1_VDD	PO	1.8/3.0 V	USIM1_VDD	PO	1.8/3.0 V	(U)SIM1 card power supply.
44	USIM_RST	DO	1.8 V	USIM1_RST	DO	1.8/3.0 V	USIM1_RST	DO	1.8/3.0 V	(U)SIM1 card reset.
45	USIM_DATA	DIO	1.8 V	USIM1_DATA	DIO	1.8/3.0 V	USIM1_DATA	DIO	1.8/3.0 V	(U)SIM1 card data.
46	USIM_CLK	DO	1.8 V	USIM1_CLK	DO	1.8/3.0 V	USIM1_CLK	DO	1.8/3.0 V	(U)SIM1 card clock.
47	USIM_GND	-	-	USIM1_GND	-	-	GND	-	-	1. Specified ground for (U)SIM card. 2. Ground.
48	GND	-	-	GND	-	-	GND	-	-	Ground.
49	ANT_GNSS	AI	-	RESERVED	-	-	ANT_GNSS	AI	-	1. GNSS antenna interface. 2. Reserved.
50	GND	-	-	GND	-	-	GND	-	-	Ground.
51	GNSS_LNA_EN	DO	1.8 V	RESERVED	-	-	GNSS_PPS	DO	1.8 V	1. External GNSS LNA enable 2. Reserved. 3. GNSS pulse per second output
52, 53	RESERVED/ VBAT_RF	PI	BG955A-GL: Voltage range ⁹ 3.3–4.3 V, Typ. 3.8 V	VBAT_RF	PI	3.3–4.3 V Typ. 3.8 V	VBAT_RF	PI	3.3–4.3 V Typ. 3.8 V	1. Reserved. 2. Power supply for the module's RF part.
54, 55	GND	-	-	GND	-	-	GND	-	-	Ground.
56	RESERVED	-	-	ANT_BT/ WIFI_SCAN ¹⁰	AIO/ AI	-	RESERVED	-	-	1. Reserved. 2. The shared antenna interface for Bluetooth and Wi-Fi Scan
57	RESERVED	-	-	RESERVED	-	-	RESERVED	-	-	1. Reserved. 2. Not connected.
58, 59	GND	-	-	GND	-	-	GND	-	-	Ground.
60	ANT_MAIN	AIO	-	ANT_MAIN	AIO	-	ANT_MAIN	AIO	-	1. BG95xA-GL & EG915U series: Main antenna interface. 2. EG91xQ family: Main antenna/Wi-Fi Scan antenna interface
61, 62	GND	-	-	GND	-	-	GND	-	-	Ground.
63	RESERVED	-	-	RESERVED	-	-	RESERVED	-	-	Reserved.
64	GPIO3	DIO	1.8 V	SPI_DOUT*	DO	1.8 V	RESERVED	-	-	1. General-purpose input/output. 2. SPI data output

¹⁰ The module supports Bluetooth and Wi-Fi Scan functions. Due to the shared antenna interface, the two functions cannot be used simultaneously. Bluetooth and Wi-Fi Scan functions are optional, and please contact Quectel Technical Support for details. Wi-Fi Scan antenna can only receive but not transmit.

											3. Reserved.
65	GPIO4	DIO	1.8 V	RESERVED	-	-	RESERVED	-	-		1. General-purpose input/output. 2. Reserved.
66	GPIO5	DIO	1.8 V	RESERVED	-	-	RESERVED	-	-		1. General-purpose input/output. 2. Reserved.
67-74	GND	-	-	GND	-	-	GND	-	-		Ground.
75	RESERVED/ GNSS_BOOT	DI	1.8 V	USB_BOOT	DI	1.8 V	USB_BOOT	DI	1.8 V		1. Reserved; force the module GNSS chip into download mode 2. Forces the module to enter download mode 3. Make the module enter download mode. Only in download mode, the module supports firmware upgrade over USB 2.0 interface.
76	RESERVED/ GNSS_NRST	DI	1.8 V	GRFC1	DO	-	GRFC1	DO	1.8 V		1. Reserved; reset the GNSS chip. 2. Generic RF controller.
77	RESERVED	-	-	GRFC2	DO	-	GRFC2	DO	1.8 V		1. Reserved. 2. Generic RF controller.
78	RESERVED	-	-	RESERVED	-	-	CAM_SPI_CLK*	DI	1.8 V		1. Reserved. 2. Camera SPI clock.
79-82	GND	-	-	GND	-	-	GND	-	-		Ground.
83	GRFC1	DO	1.8 V	USIM2_DET	DI	1.8 V	RESERVED	-	-		1. Generic RF controller. 2. (U)SIM2 card hot-plug detect. 3. Reserved.
84	GRFC2	DO	1.8 V	USIM2_CLK	DO	1.8/3.0 V	USIM2_CLK ¹¹	DO	1.8 V		1. Generic RF controller. 2. (U)SIM2 card clock.
85	GPIO6	DIO	1.8 V	USIM2_RST	DO	1.8/3.0 V	USIM2_RST ¹¹	DO	1.8 V		1. General purpose input/output. 2. (U)SIM2 card reset.
86	GPIO7	DIO	1.8 V	USIM2_DATA	DIO	1.8/3.0 V	USIM2_DATA ¹¹	DIO	1.8 V		1. General purpose input/output. 2. (U)SIM2 card data.
87	GPIO8	DIO	1.8 V	USIM2_VDD	PO	1.8/3.0 V	USIM2_VDD ¹¹	PO	1.8 V		1. General purpose input/output. 2. (U)SIM2 card power supply.
88	GPIO9	DIO	1.8 V	SPI_DIN*	DI	1.8 V	RESERVED	-	-		1. General purpose input/output. 2. SPI data input. 3. Reserved.
89-91	GND	-	-	GND	-	-	GND	-	-		Ground.
92	RESERVED	-	-	RESERVED	-	-	RESERVED	-	-		Reserved.
93	RESERVED	-	-	RESERVED	-	-	CAM_VDDIO*	PO	1.8 V		1. Reserved. 2. Camera digital power supply.
94	CLI_RXD/ CLI_RXD2	DI	1.8 V	RESERVED	-	-	CAM_VDD*	PO	2.8 V		1. CLI UART receive/ CLI UART2 receive 2. Reserved.

¹¹ For EG91xQ family, USIM2 and Camera SPI* cannot be used at the same time.

											3. Camera analog power supply.
95	CLI_TXD/ CLI_TXD2	DO	1.8 V	RESERVED	-	-	CAM_MCLK*	DO	1.8 V		1. CLI UART transmit/CLI UART2 transmit. 2. Reserved. 3. Master clock of the camera.
96	PON_TRIG ¹²	DI	1.8 V	PSM_EINT	-	-	PSM_INT*	DI	1.8 V		1. Used for main UART function control and for entering/exiting e-I-DRX, PSM or sleep modes 2. Wake up the module from power saving mode.
97	RESERVED/ GNSS_EN	DI	1.8 V	RESERVED	-	-	CAM_SPI_DATA0*	DI	1.8 V		1. Enable internal GNSS chip. 2. Reserved. 3. Camera SPI data bit 0.
98	RESERVED/ SFNIND_1PPS	DO	1.8 V	RESERVED	-	-	CAM_SPI_DATA1*	DI	1.8 V		1. One pulse per second. 2. Reserved. 3. Camera SPI data bit 1.
99	VDD_RF	PO	1.8 V	RESERVED	-	-	RESERVED	-	-		1. External GNSS LNA power supply. 2. Reserved.
100–102	GND	-	-	GND	-	-	GND	-	-		Ground.
103–106	-	-	-	RESERVED	-	-	RESERVED	-	-		Reserved.
107–108	-	-	-	RESERVED	-	-	RESERVED	-	-		Reserved.
109	-	-	-	RESERVED	-	-	GNSS_DBG_TXD	DO	1.8 V		GNSS debug UART transmit.
110	-	-	-	RESERVED	-	-	GNSS_DBG_RXD	DI	1.8 V		GNSS debug UART receive.
111	-	-	-	RESERVED	-	-	RESERVED	-	-		Reserved.
112	-	-	-	RESERVED	-	-	GNSS_RST	DI	1.8 V		Reset the GNSS chip
113, 114	-	-	-	RESERVED	-	-	RESERVED	-	-		Reserved.
115	-	-	-	RESERVED	-	-	CAM_PWDN*	DO	1.8 V		Power down of the camera
116	-	-	-	RESERVED	-	-	RESERVED	-	-		Reserved.
117	-	-	-	RESERVED	-	-	GNSS_PWR_EN	DI	1.8 V		GNSS power enabled.
118	-	-	-	RESERVED	-	-	GNSS_VBCKP	PI	1.9–3.6 V Typ. 3.3 V		Power supply for GNSS RTC.
119	-	-	-	MIC_N	AI	-	RESERVED	-	-		1. Microphone analog input (-) 2. Reserved.
120	-	-	-	MICBIAS	PO	-	RESERVED	-	-		Bias voltage output for microphone Reserved.
121	-	-	-	SPK_P	AO	-	RESERVED	-	-		Analog audio differential output (+)

¹² On the module without PON_TRIG function, this pin has no function and there is no need to design it. For the module's PON_TRIG difference, see **document [1]**.

										Reserved.
122	-	-	-	SPK_N	AO	-	RESERVED	-	-	Analog audio differential output (-) Reserved.
123	-	-	-	HP_L	AO	-	RESERVED	-	-	Headphone left channel output Reserved.
124	-	-	-	HP_R	AO	-	RESERVED	-	-	Headphone right channel output Reserved.
125	-	-	-	HP_DET	DI	-	RESERVED	-	-	Headphone hot-plug detect Reserved.
126	-	-	-	MIC_P	AI	-	RESERVED	-	-	Microphone analog input (+) Reserved.

NOTE

1. Pins 103–126 in **purple** are additional pins on EG915U series and EG91xQ family that are not available on BG95xA-GL.
2. Pins in **blue** are pins with different functions or voltage domain on BG95xA-GL, EG915U series and EG91xQ family, but the module footprint is compatible.
3. Pins in **black** are compatible pins on BG95xA-GL, EG915U series and EG91xQ family with the same functionality.
4. Pins 27, 28, 33, 52, 53, 75, 76, 94, 95, 97 and 98 have different functions on BG950A-GL, BG951A-GL and BG955A-GL. For more details, see **document [1]**.
5. **BG95xA-GL:**
 - 1) For every VBAT transition/re-insertion from 0 V, VBAT slew rate < 25 mV/μs. To ensure normal module startup, pulling down PWRKEY to turn on the module after VBAT remains stable for 100 ms.
 - 2) After entering PSM or turn-off mode, it is prohibited to provide any external voltage to the module's I/O ports that are not defined as a wake-up source.

4 Hardware Interface Design

4.1. Power Supply

Table 8: Pin Difference of VBAT_BB & VBAT_RF

Pin Name	DC Characteristics		
	BG95xA-GL	EG915U Series	EG91xQ Family
VBAT_BB	BG950A-GL/ BG951A-GL: Voltage range ⁸ : 2.2–4.35 V, Typ. 3.3 V I _{max} = 0.8 A	V _{max} = 4.3 V V _{min} = 3.3 V V _{nom} = 3.8 V	V _{max} = 4.3 V V _{min} = 3.3 V V _{nom} = 3.8 V
VBAT_RF	BG955A-GL: Voltage range ⁹ 3.3–4.3 V, Typ. 3.8 V I _{max} = 2.3 A	VBAT_BB: I _{max} = 1 A VBAT_RF: I _{max} = 2.5 A	VBAT_BB: I _{max} = 0.3 A VBAT_RF: I _{max} = 1.2 A

NOTE

For BG95xA-GL, the pin number of VBAT_BB and VBAT_RF is different. For more details, see [document \[1\]](#).

- **BG95xA-GL**

To ensure power supply stability, it is necessary to add two high-power TVS components near VBAT_BB and VBAT_RF.

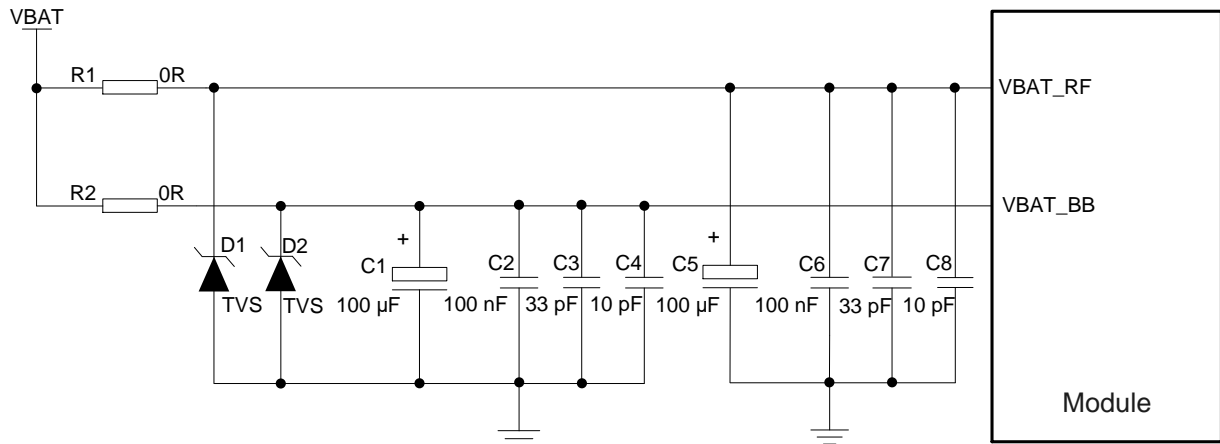


Figure 2: Power Supply in Star Structure (BG95xA-GL)

● **EG915U & EG91xQ Family**

To avoid the ripple and surge and to ensure the stability of the power supply to the module, it is recommended to add a TVS with $V_{RWM} = 4.7\text{ V}$, low clamping voltage and high reverse peak pulse current I_{pp} at the front end of the power supply.

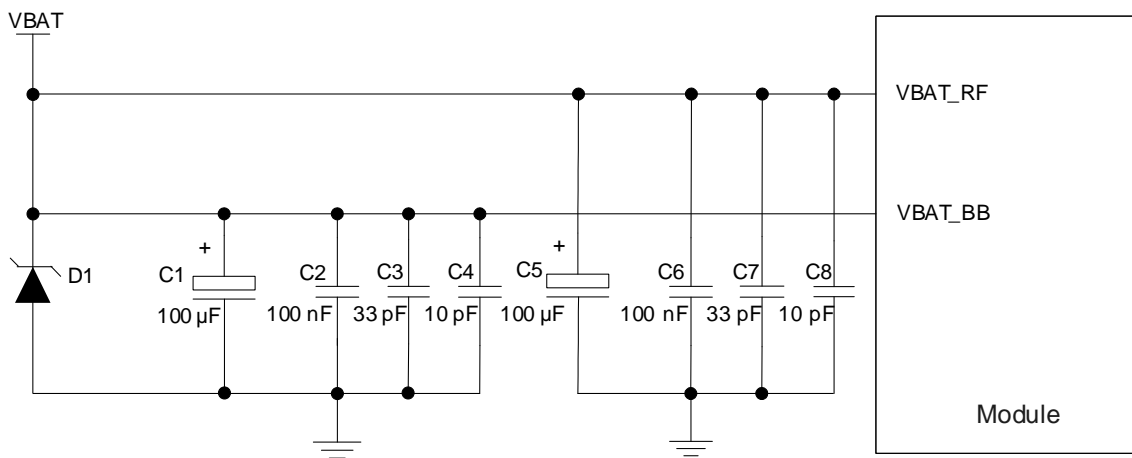


Figure 3: Power Supply in Star Structure (EG915U & EG91xQ Family)

4.2. Turn-on/off

The turn-on/off methods are the same for BG95xA-GL, EG915U series and EG91xQ family. The modules can be turned on or turned off after pressing PWRKEY for a certain time.

4.2.1. Turn-on

Turn-on circuits of the modules are presented in the figures below.

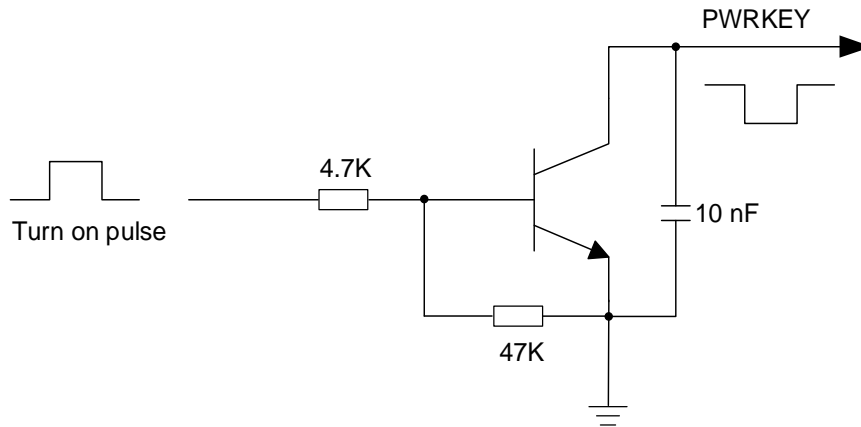


Figure 4: Turn On Modules with a Driving Circuit

Table 9: Timing of Turn-on Pulse

Module	Timing of Turn-on Pulse
BG95xA-GL	500–1000 ms
EG915U Series	≥ 2 s
EG91xQ Family	≥ 500 ms

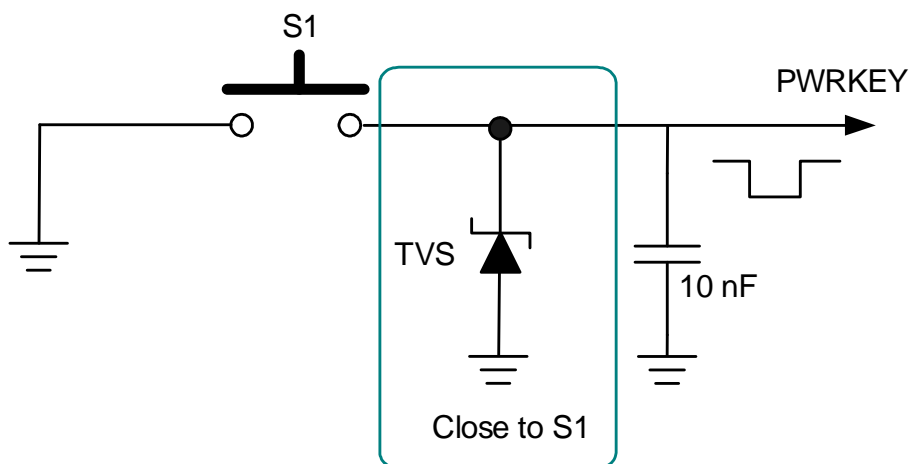


Figure 5: Turn On Modules with a Button

● **BG95xA-GL**

When the module is in turn-off mode, driving PWRKEY low for 500–1000 ms and then releasing it will turn on the module. It is recommended to use an open drain/collector driver to control PWRKEY.

BG95xA-GL has models with PON_TRIG and models without PON_TRIG. The turn-on timing and requirements have slight differences between these two versions. This chapter mainly illustrates the turn-on requirements of models with PON_TRIG. For more information, see **document [1]**.

Drive PWRKEY low after VBAT is stable for 100–200 ms, the module will be turned on immediately.

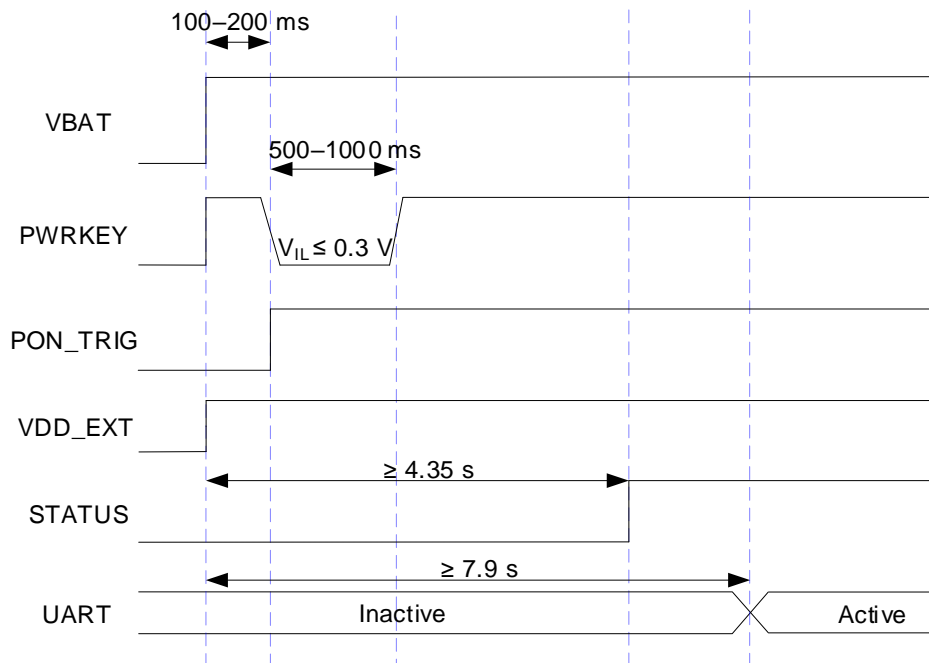


Figure 6: Turn-on Timing With PON_TRIG (After VBAT is Stable for 100–200 ms)

NOTE

Ensure that VBAT is stable for 100–200 ms before pulling down PWRKEY.

Drive PWRKEY low after VBAT is stable for more than 250 ms, the module will be turned on immediately.

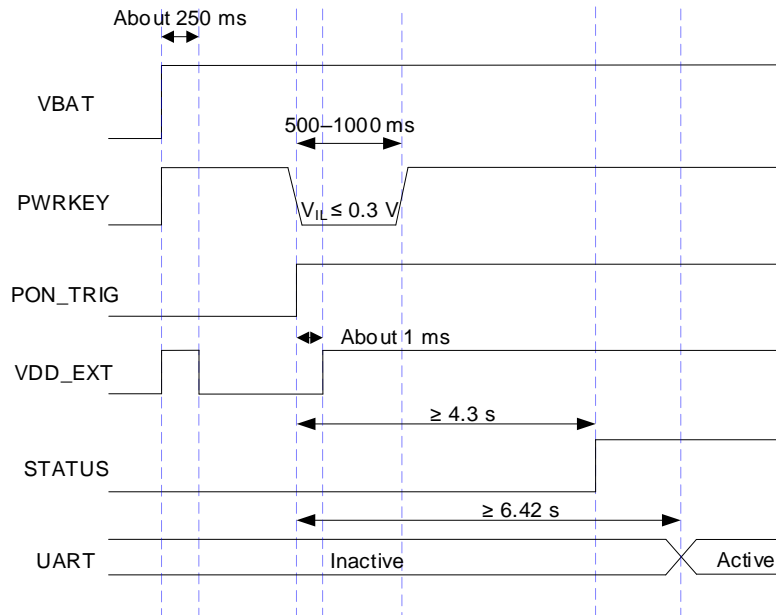


Figure 7: Turn-on Timing With PON_TRIG (After VBAT is Stable for More Than 250 ms)

NOTE

After VBAT is powered up, it will take about 250 ms for the module to load the internal program.

● **EG915U Series**

If the module needs to turn on automatically, PWRKEY can be driven low directly to ground with a recommended resistor less than 1 kΩ. However, ensure that the voltage of VBAT_BB and VBAT_RF pins is below 0.5 V before power-up.

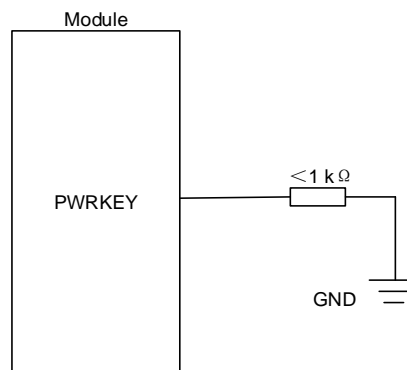


Figure 8: Turning On the Module Automatically

When the module is in turn-off mode, you can turn it on to normal mode by driving the PWRKEY pin low for at least 2 s. It is recommended to use an open drain/collector driver to control the PWRKEY.

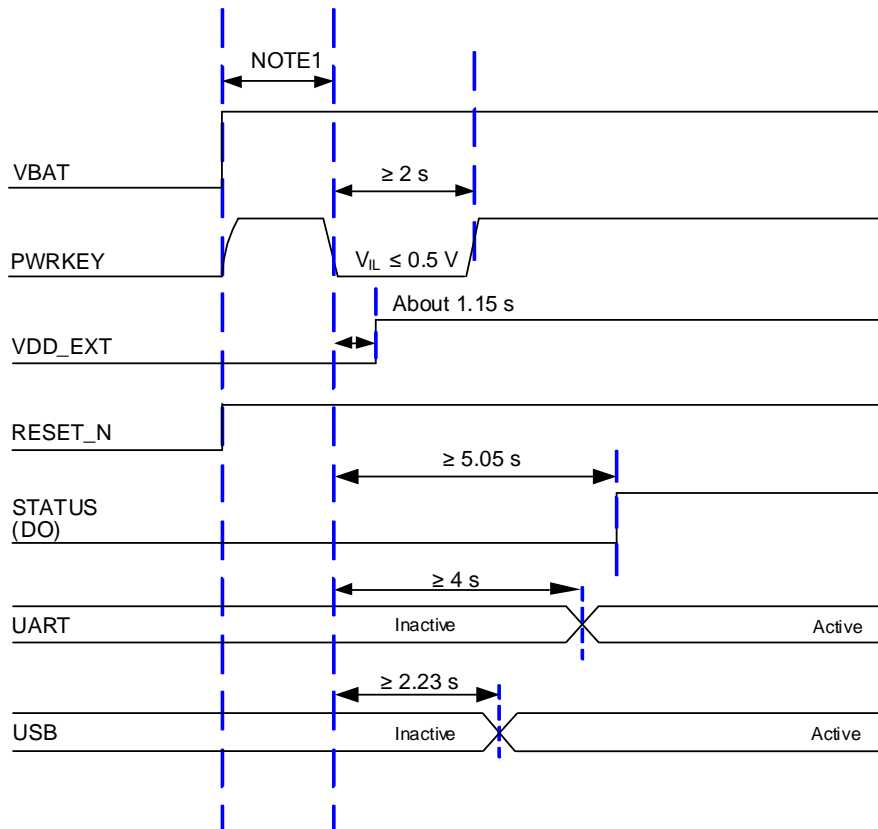


Figure 9: Turn-on Timing with PWRKEY (EG915U Series)

NOTE

1. Before pulling down the PWRKEY, ensure that the VBAT voltage is stable within the recommended range of 3.3–4.3 V. Ensure the voltage of VBAT is stable for at least 30 ms before driving the PWRKEY low.
2. When PWRKEY is connected to GND with a pull-down resistor, the module will not boot automatically after being turned off with the AT command. In this case, it is necessary to forcibly disconnect the VBAT power supply and power up the module again. Therefore, it is recommended to use a control circuit to control the PWRKEY to turn on/off the module.
3. Ensure that the VBAT voltage is less than 0.5 V before powering up the module again. If MOSFET is used to control the VBAT power supply, a discharge circuit must be designed to ensure that the VBAT voltage can be released quickly after the module is turned off and powered down.
4. Pay special attention to the following two turn-on scenarios:
 - 1) In the scenario where USB_VBUS is connected first (or has always been connected), VBAT is powered up later, and then PWRKEY is pulled down to start up the module, it is necessary to ensure that VBAT is powered up stably for at least 2 s before PWRKEY is pulled down;
 - 2) In the scenario where VBAT is powered up first (or has always been powered up), USB_VBUS is connected later, and then PWRKEY is pulled down to start up the module, it is necessary to ensure that USB_VBUS is connected for at least 2 s before PWRKEY is pulled down.

4.3. Turn-off

- **EG91xQ Family**

When the module is in turn-off mode, it can be turned on by driving the PWRKEY low for at least 500 ms. It is recommended to use an open drain/collector driver to control the PWRKEY.

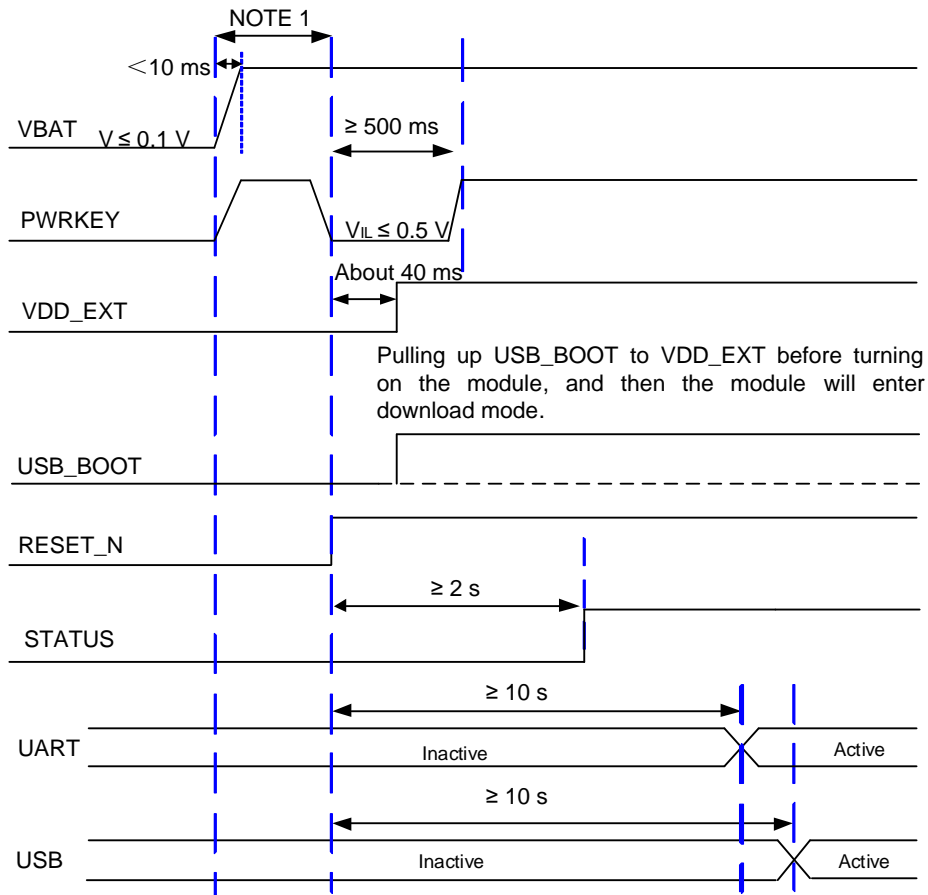


Figure 10: Turn-on Timing with PWRKEY (EG91xQ Family)

NOTE

1. Ensure the voltage of VBAT is stable for at least 30 ms before driving the PWRKEY low.
2. If the module needs to turn on automatically but does not need the turn-off function, PWRKEY can be driven low directly to ground with a recommended 4.7 kΩ resistor.

4.3.1. Turn-off

4.3.1.1. Turn Off with PWRKEY

● **BG95xA-GL**

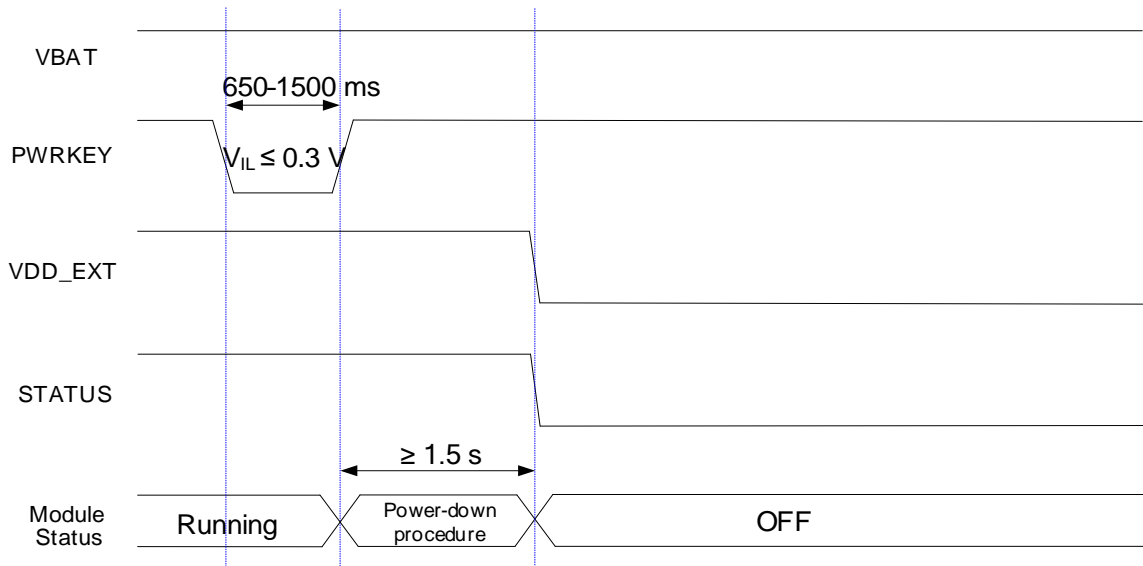


Figure 11: Turn-off Timing (BG95xA-GL)

● **EG915U Series & EG91xQ Family**

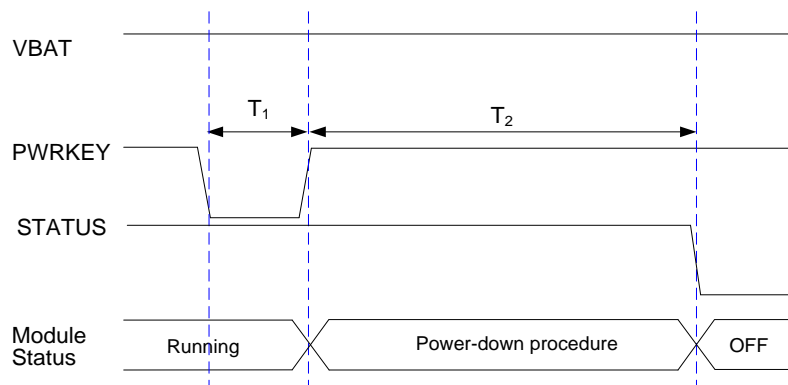


Figure 12: Turn-off Timing (EG915U & EG91xQ Family)

Table 10: Power-down Timing with PWRKEY

Module	T_1	T_2
EG915U Series	$\geq 3s$	$\geq 30s$
EG91xQ Family	$\geq 650ms$	$\geq 1.35s$

4.3.1.2. Turn Off with AT Command

The modules can also be safely turned off with **AT+QPOWD**, which is similar to turning off the modules via PWRKEY pin. See **documents [4], [5], and [6]** for details about **AT+QPOWD**.

NOTE

1. To avoid corrupting the data in the internal flash, do not switch off the power supply while the module is working normally. The power supply can be cut off only after the module is shut down with PWRKEY or AT command.
2. **BG95xA-GL:** When the module is turned off with AT command, keep PWRKEY at a high level after executing the power-off command. Otherwise, the module will be turned on again after turn-off.
3. **EG915U series:** When being turned off, the module will log out of the network. The time for logging out relates to its network status. Thus, please pay attention to the shutdown time in your design because the actual shutdown time varies according to the network status.
4. **EG91xQ family:**
 - 1) If the module is turned on by connecting the PWRKEY to ground for a long time, **AT+QPOWD** cannot be used to turn off the module.
 - 2) When turning off the module with the AT command, keep PWRKEY at high level after the execution of the command. Otherwise, the module cannot be turned off successfully.

4.4. Reset

- **BG95xA-GL & EG915U Series**

BG95xA-GL and EG915U series can be reset by driving RESET_N low for a certain time or directly via a button.

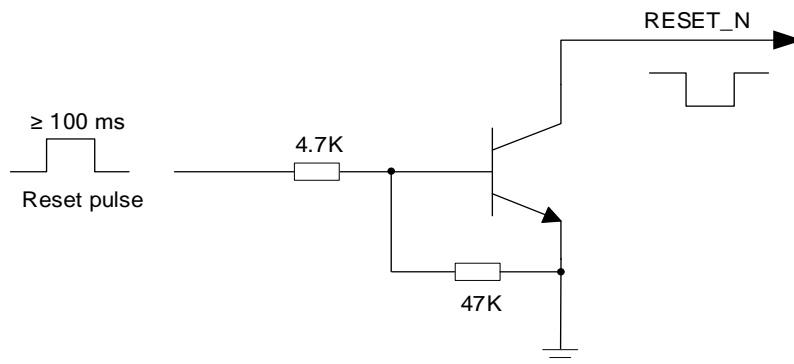


Figure 13: Reference Design of RESET_N with a Driving Circuit (BG95xA-GL & EG915U Series)

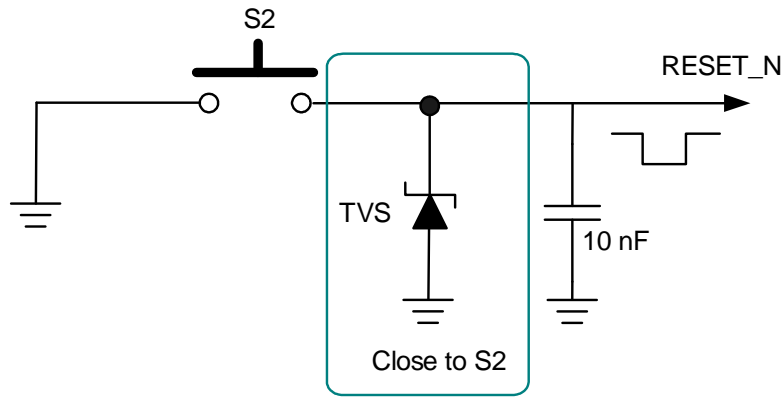


Figure 14: Reference Circuit of RESET_N by Using a Button (BG95xA-GL & EG915U Series)

The reset timing for BG95xA-GL and EG915U series is illustrated in the following figure.

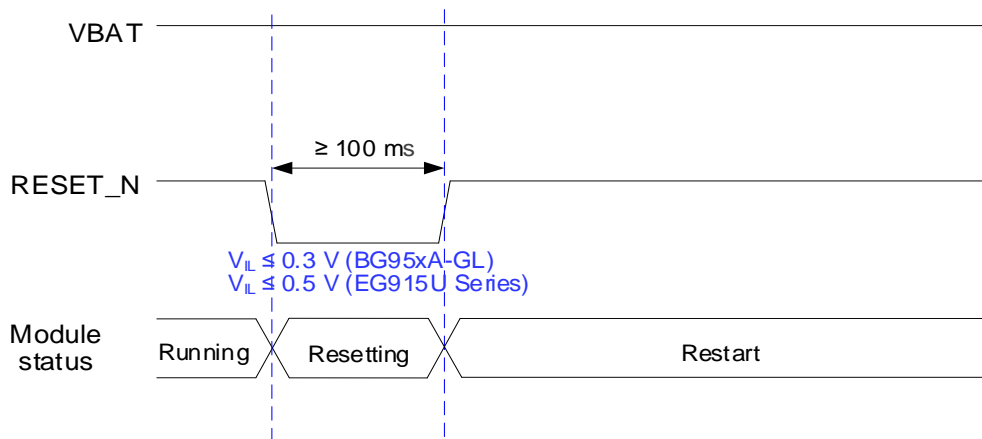


Figure 15: Reset Timing (BG95xA-GL & EG915U Series)

NOTE

1. Ensure that there is no large capacitance on RESET_N pins.
2. **BG95xA-GL:** Because PWRKEY and RESET traces are sensitive signal traces, it's necessary to surround the traces with ground on that layer and with ground planes above and below, and keep their traces away from each other, so as to reduce interference.
3. **EG915U series:**
 - 1) The RESET_N pin performs a soft reset which only resets the baseband, not the PMU.
 - 2) It is recommended to use RESET_N only when you fail to turn off the module with the **AT+QPOWD** or PWRKEY pin.

● **EG91xQ Family**

For EG91xQ family, the reset function is activated by using both the PWRKEY and RESET_N pins. The module can be reset by pulling down PWRKEY when RESET_N is at low level.

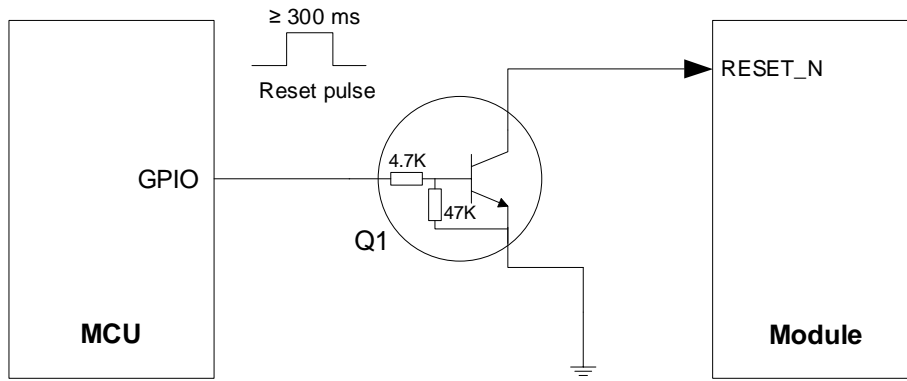


Figure 16: Reference Design of Reset with a Driving Circuit (EG91xQ Family)

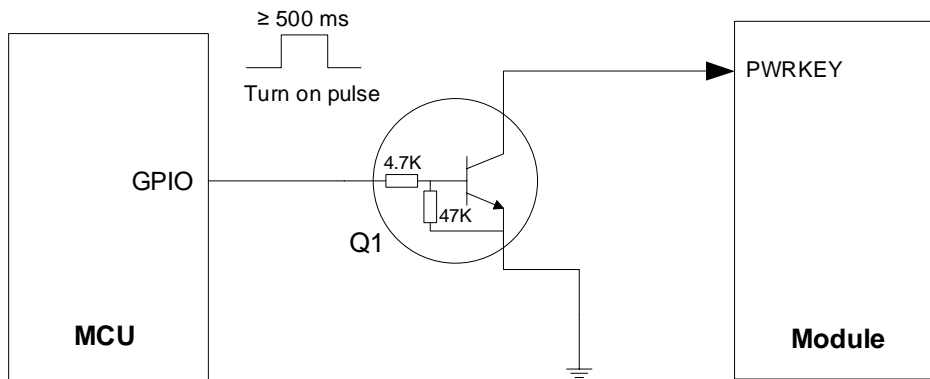


Figure 17: Reference Design of PWRKEY with a Driving Circuit (EG91xQ Family)

The reset timing for EG91xQ family is illustrated in the following figure.

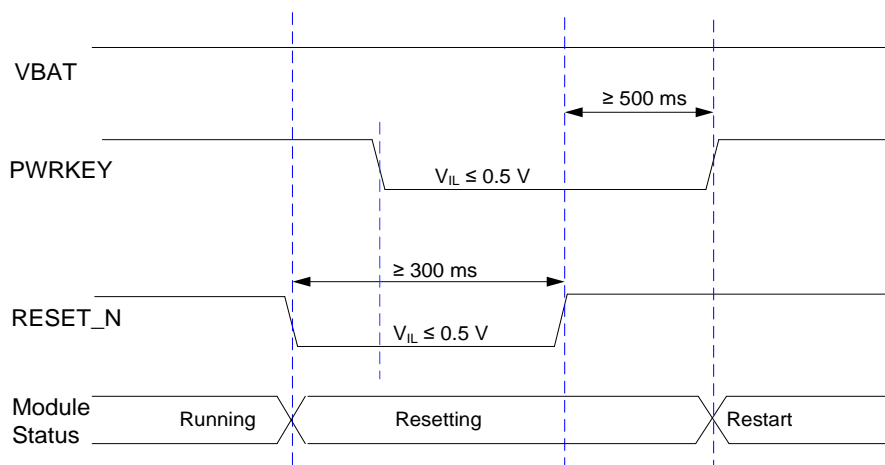


Figure 18: Reset Timing (EG91xQ Family)

NOTE

1. Ensure that there is no large capacitance on PWRKEY and RESET_N pins.
2. In reset timing, pull down PWRKEY when RESET_N is at low level.

4.5. (U)SIM Interfaces

- BG95xA-GL: **one** (U)SIM interface
- EG915U & EG91xQ families: **two** (U)SIM interfaces.

Table 11: Pin Difference of (U)SIM Interfaces

Pin No.	BG95xA-GL	EG915U Series	EG91xQ Family	Comment
42	USIM_DET	USIM1_DET	USIM1_DET	1.8 V power domain.
43	USIM_VDD	USIM1_VDD	USIM1_VDD	BG95xA-GL: Only 1.8 V (U)SIM card is supported.
44	USIM_RST	USIM1_RST	USIM1_RST	
45	USIM_DATA	USIM1_DATA	USIM1_DATA	EG915U & EG91xQ families: Either 1.8 V or 3.0 V (U)SIM card is supported and can be identified automatically by the module.
46	USIM_CLK	USIM1_CLK	USIM1_CLK	
47	USIM_GND	USIM1_GND	GND	-
83	-	USIM2_DET	-	1.8 V power domain.
84	-	USIM2_CLK	USIM2_CLK	EG915U series: 1.8 V or 3.0 V (U)SIM2 card is supported.
85	-	USIM2_RST	USIM2_RST	
86	-	USIM2_DATA	USIM2_DATA	EG91xQ family: USIM2 interface only supports 1.8 V power domain.
87	-	USIM2_VDD	USIM2_VDD	

NOTE

EG91xQ family:

1. When USIM1 and USIM2 are used at the same time, the power domain of USIM interfaces should

be 1.8 V. Otherwise, USIM2 interface will be damaged.

2. USIM2 and Camera SPI* cannot be used at the same time.

4.6. USB Interface

BG95xA-GL, EG915U series and EG91xQ family provide one integrated Universal Serial Bus (USB) interface, which complies with USB 2.0 specification and only supports USB slave mode.

Table 12: Data Rate and Function of USB Interface

Module	Data Rate	Function
BG95xA-GL	<ul style="list-style-type: none"> ● Full-speed (12 Mbps) 	<ul style="list-style-type: none"> ● AT command communication ● Data transmission ● Software debugging ● Firmware upgrade*
EG915U series	<ul style="list-style-type: none"> ● High-speed (480 Mbps) ● Full-speed (12 Mbps) 	<ul style="list-style-type: none"> ● AT command communication ● Data transmission ● Software debugging ● Firmware upgrade
EG91xQ family	<ul style="list-style-type: none"> ● High-speed (480 Mbps) ● Full-speed (12 Mbps) 	<ul style="list-style-type: none"> ● AT command communication ● Data transmission ● Software debugging ● Firmware upgrade ● GNSS NMEA sentence output (All-in-one mode only) ● Partial log output

NOTE

The GNSS function for EG91xQ family is optional.

Table 13: Pin Difference of USB_VBUS

Pin Name	Pin No.	I/O	DC Characteristics		
			BG95xA-GL	EG915U Series	EG91xQ Family
USB_VBUS	8	AI	Vnom = 5.0 V	Vmax = 5.25 V Vmin = 3.5 V	Vmax = 5.25 V Vmin = 3.0 V

Vnom = 5.0 V

Vnom = 5.0 V

For BG95xA-GL, it is recommended to reserve test points for USB interface.

For EG915U series and EG91xQ family, test points of USB interface must be reserved.

Following figures illustrate the reference design of USB interface.

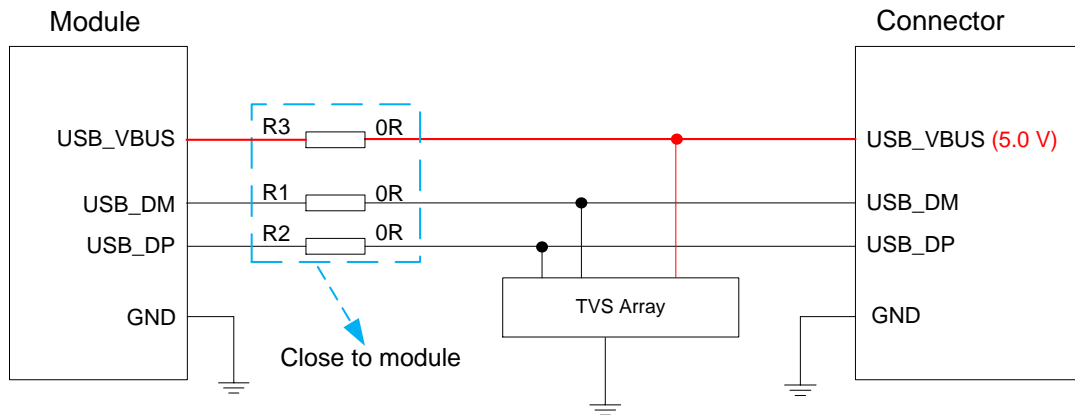


Figure 19: Reference Design of USB Interface (BG95xA-GL)

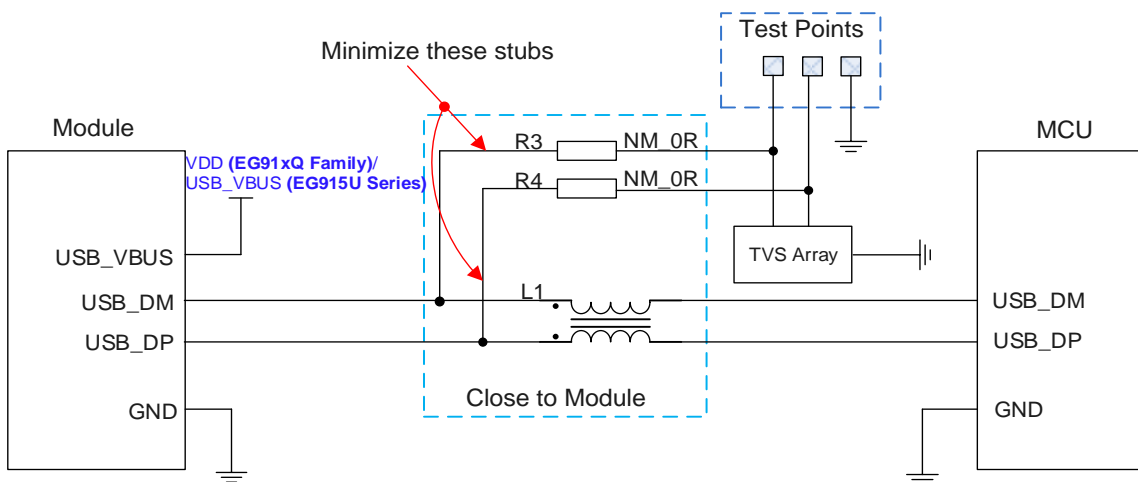


Figure 20: Reference Design of USB Interface (EG915U & EG91xQ Families)

4.7. UART Interfaces

UART interfaces supported by BG95xA-GL, EG915U series and EG91xQ family are listed below.

Table 14: Supported UART Interfaces

Modules	UART Interfaces
BG95xA-GL	1. Main UART 2. Debug UART 3. GNSS UART (Only BG951A-GL) 4. CLI UART
EG915U series	1. Main UART 2. Debug UART 3. Auxiliary UART
EG91xQ family	1. Main UART 2. Debug UART 3. GNSS UART 4. GNSS debug UART

Table 15: Pin Difference of UART Interfaces

UART	Pin No.	BG95xA-GL	EG915U Series	EG91xQ Family
Main UART	30	MAIN_DTR	MAIN_DTR	MAIN_DTR
	34	MAIN_RXD	MAIN_RXD	MAIN_RXD
	35	MAIN_TXD	MAIN_TXD	MAIN_TXD
	36	MAIN_CTS	MAIN_CTS	MAIN_CTS
	37	MAIN_RTS	MAIN_RTS	MAIN_RTS
	38	MAIN_DCD	MAIN_DCD	MAIN_DCD
	39	MAIN_RI	MAIN_RI	MAIN_RI
Debug UART	22	DBG_RXD	DBG_RXD	DBG_RXD
	23	DBG_TXD	DBG_TXD	DBG_TXD
Auxiliary UART/ GNSS UART/ CLI UART	27	CLI_TXD1/ GNSS_TXD	AUX_TXD	GNSS_TXD
	28	CLI_RXD1/ GNSS_RXD	AUX_RXD	GNSS_RXD
	94	CLI_RXD/ CLI_RXD2	-	-
	95	CLI_TXD/ CLI_TXD2	-	-

GNSS debug UART	110	-	-	GNSS_DBG_RXD
	109	-	-	GNSS_DBG_TXD

NOTE

1. For EG91xQ family, GNSS UART and GNSS debug UART interfaces are optional. If you need these functions, please contact Quectel Technical Support.
2. Pins 27, 28, 94 and 95 have different functions on BG950A-GL, BG951A-GL and BG955A-GL. For more details, see **document [1]**.

4.8. Antenna Interfaces

The supported antenna interfaces of BG95xA-GL, EG915U series and EG91xQ family are listed below.

Table 16: Pin Definition of Antenna Interfaces

Pin No.	I/O	BG95xA-GL	EG915U Series	EG91xQ Family	Comment
49	AI	ANT_GNSS	-	ANT_GNSS	50 Ω impedance.
60	AIO	ANT_MAIN	ANT_MAIN	ANT_MAIN	50 Ω impedance. BG95xA-GL & EG915U series: Main antenna interface. EG91xQ family: Main antenna/ Wi-Fi Scan antenna interface
56	AIO/ AI	-	ANT_BT/ WIFI_SCAN	-	50 Ω impedance. Wi-Fi Scan can only receive but not transmit.

NOTE

For EG915U series, due to the shared antenna interface, the two functions cannot be used simultaneously. Bluetooth and Wi-Fi Scan functions are optional, and please contact Quectel Technical Support for details.

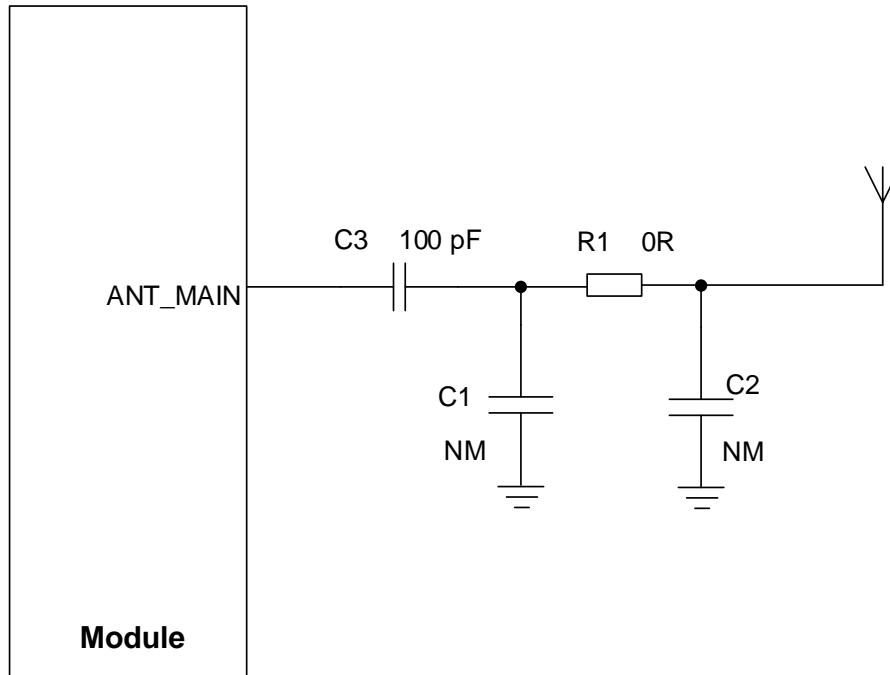


Figure 21: ANT_MAIN Reference Design (BG95xA-GL & EG91xQ Families)

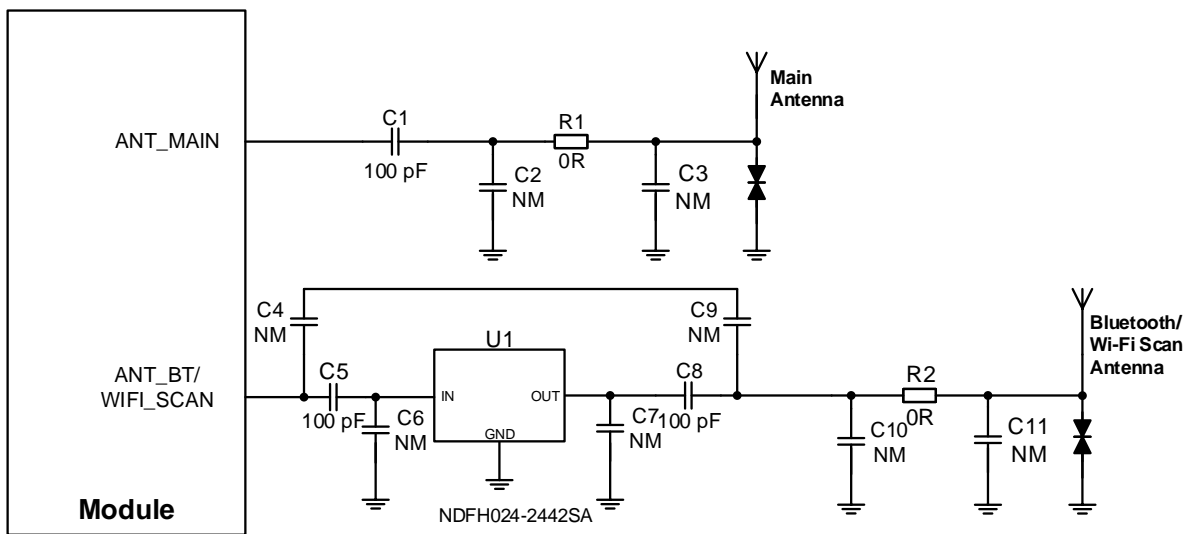


Figure 22: RF Antennas Reference Circuit (EG915U Series)

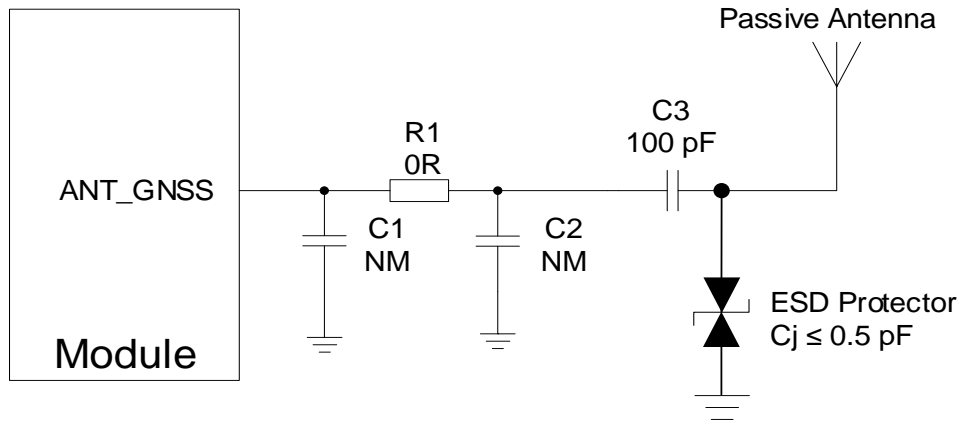


Figure 23: GNSS Antenna Reference Design (BG95xA-GL)

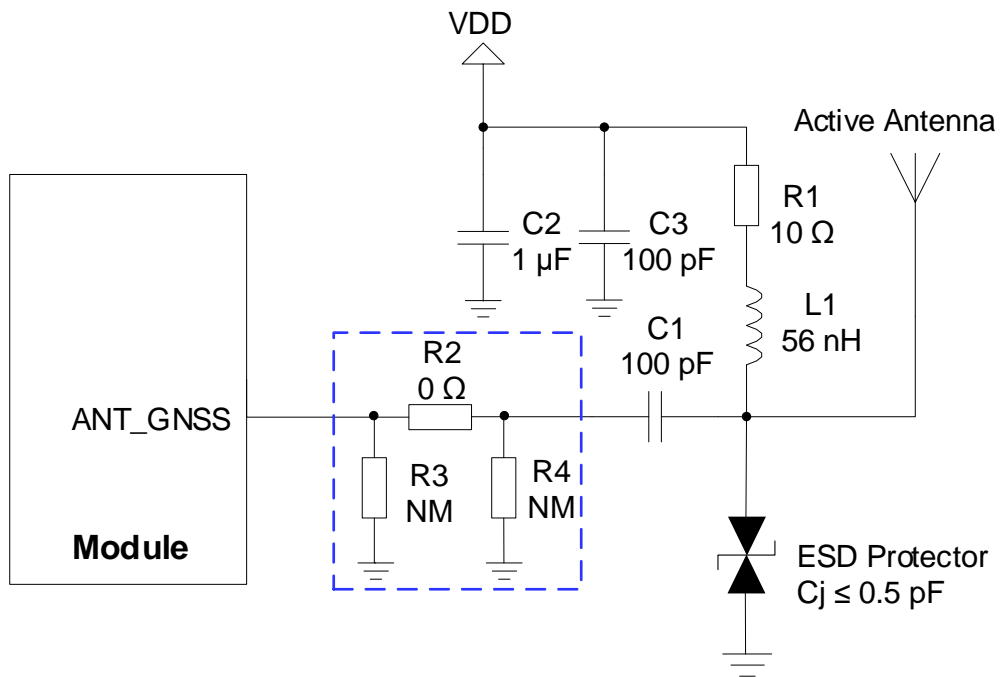


Figure 24: GNSS Antenna Reference Design (EG91xQ Family)

For more details about antenna reference design, see **document [1], [2] and [3]**.

NOTE

1. ANT_GNSS of EG91xQ family is optional.
2. BG95xA-GL is designed with a built-in LNA, and supports passive GNSS antennas only. Active antennas and external LNAs are not supported.

5 Recommended Footprint

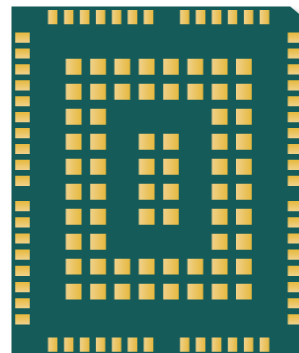
This chapter primarily describes the recommended footprint and stencil design for BG95xA-GL, EG915U series and EG91xQ family. All dimensions are measured in mm, and the dimensional tolerances are ± 0.2 mm.

5.1. Recommended Compatible Footprint

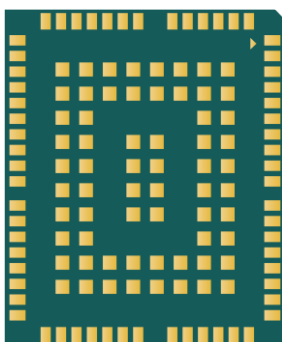
The following figure shows the bottom views of the modules.



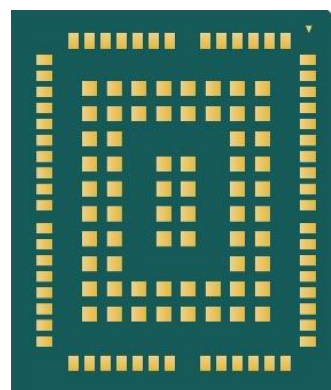
BG95xA-GL



EG915U Series



EG915Q-NA



EG916Q-GL

Figure 25: Bottom Views

NOTE

Images above are for illustrative purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Quectel.

The following figure shows the recommended compatible footprint of BG95xA-GL, EG915U series and EG91xQ family.

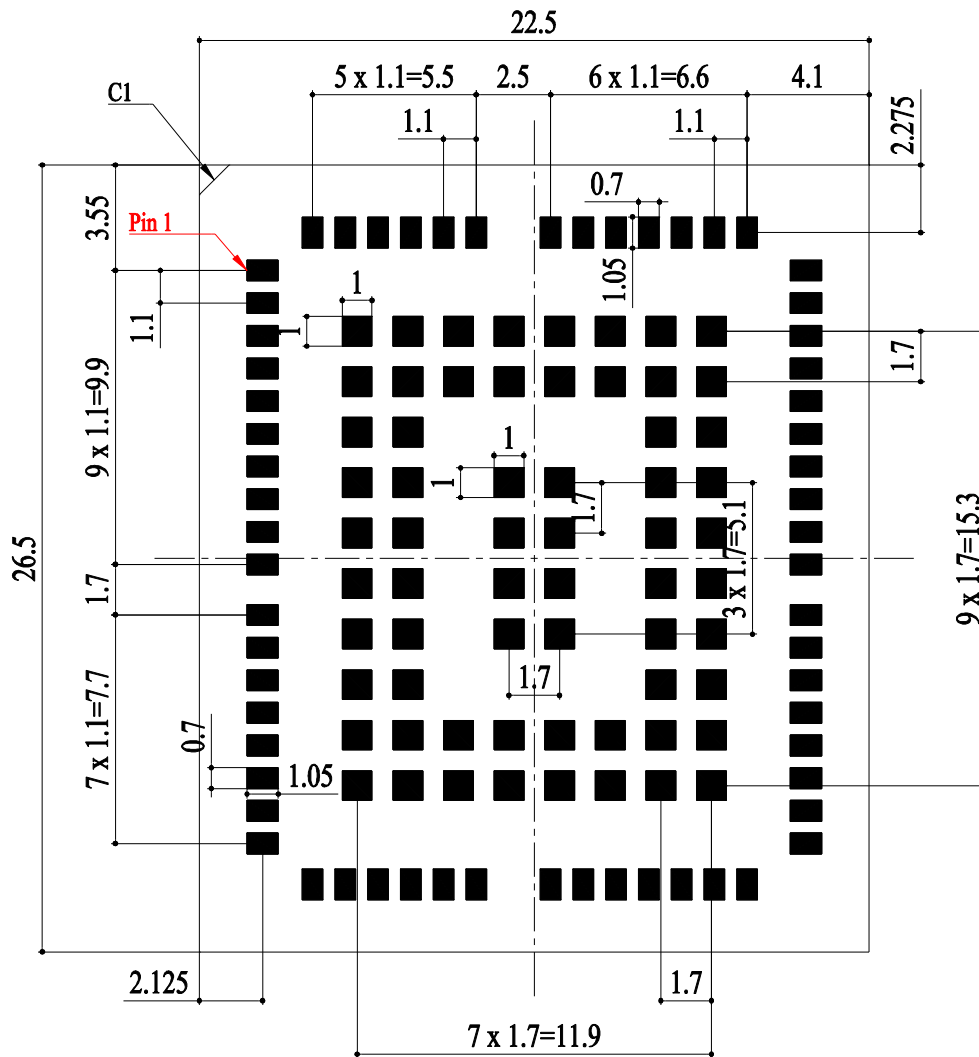


Figure 26: Recommended Compatible Footprint

NOTE

1. The module's coplanarity standard: ≤ 0.13 mm.
2. Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.

5.2. Installation Sketch Map

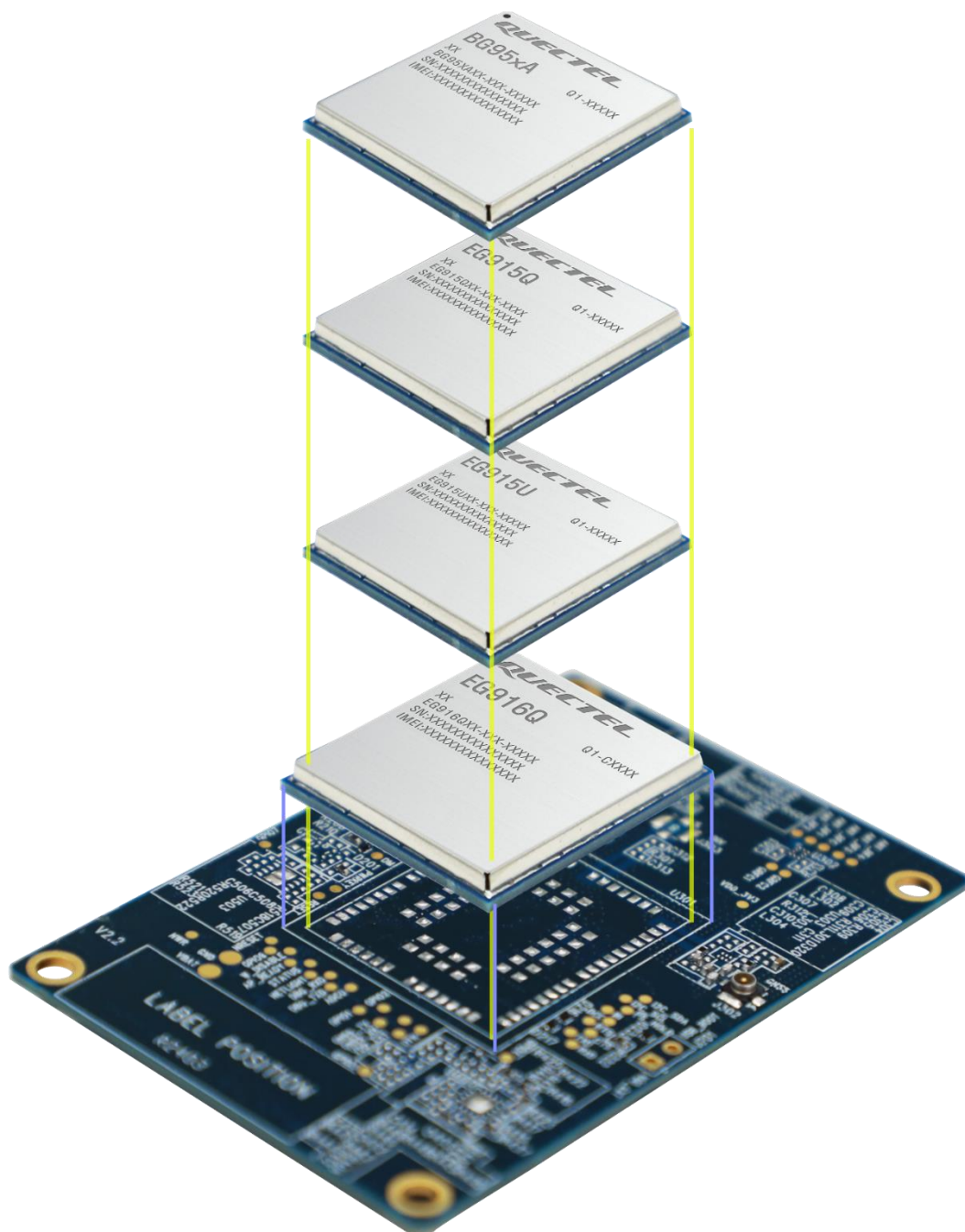


Figure 27: Installation Sketch Map

6 Appendix References

Table 17: Related Documents

Document Name
[1] Quectel_BG95xA-GL_Hardware_Design
[2] Quectel_EG91xQ_Series_Hardware_Design
[3] Quectel_EG915U_Series_Hardware_Design
[4] Quectel_BG77xA-GL&BG95xA-GL_AT_Commands_Manual
[5] Quectel_EC200U&EG800G&EG91xU&EG915G_Series_AT_Commands_Manual
[6] Quectel_EG800Q&EG91xQ_Series_AT_Commands_Manual

Table 18: Terms and Abbreviations

Abbreviation	Description
bps	bits per second
CTS	Clear To Send
DFOTA	Delta Firmware Upgrade Over The Air
DRX	Discontinuous Reception
DTR	Data Terminal Ready
FDD	Frequency Division Duplex
GNSS	Global Navigation Satellite System
GPRS	General Packet Radio Service
GSM	Global System for Mobile Communications

HSDPA	High Speed Downlink Packet Access
I _{max}	Maximum Load Current
I/O	Input/Output
IoT	Internet of Things
LGA	Land Grid Array
LPWA	Low-Power Wide-Area (Network)
LTE	Long Term Evolution
NMEA	NMEA (National Marine Electronics Association) 0183 Interface Standard
PCM	Pulse Code Modulation
PSM	Power Saving Mode
RF	Radio Frequency
SMS	Short Message Service
TDD	Time Division Duplexing
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
(U)SIM	(Universal) Subscriber Identity Module
V _{max}	Maximum Voltage
V _{nom}	Nominal Voltage
V _{min}	Minimum Voltage
