L26-LB

Reference Design

GNSS Module Series

Rev. L26-LB_Reference_Design_V1.2

Date: 2020-05-14

Status: Released

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About the Document

Revision History

Version	Date	Author	Description
1.0	2020-03-18	Ronnie HU/ Phil GAO	Initial
1.1	2020-04-29	Ronnie HU	Changed U301 from ADCMP370AKSZ-REEL7 to ADCMP371AKSZ-REEL7.
1.2	2020-05-14	Phil GAO	Updated the recommended value of R301.

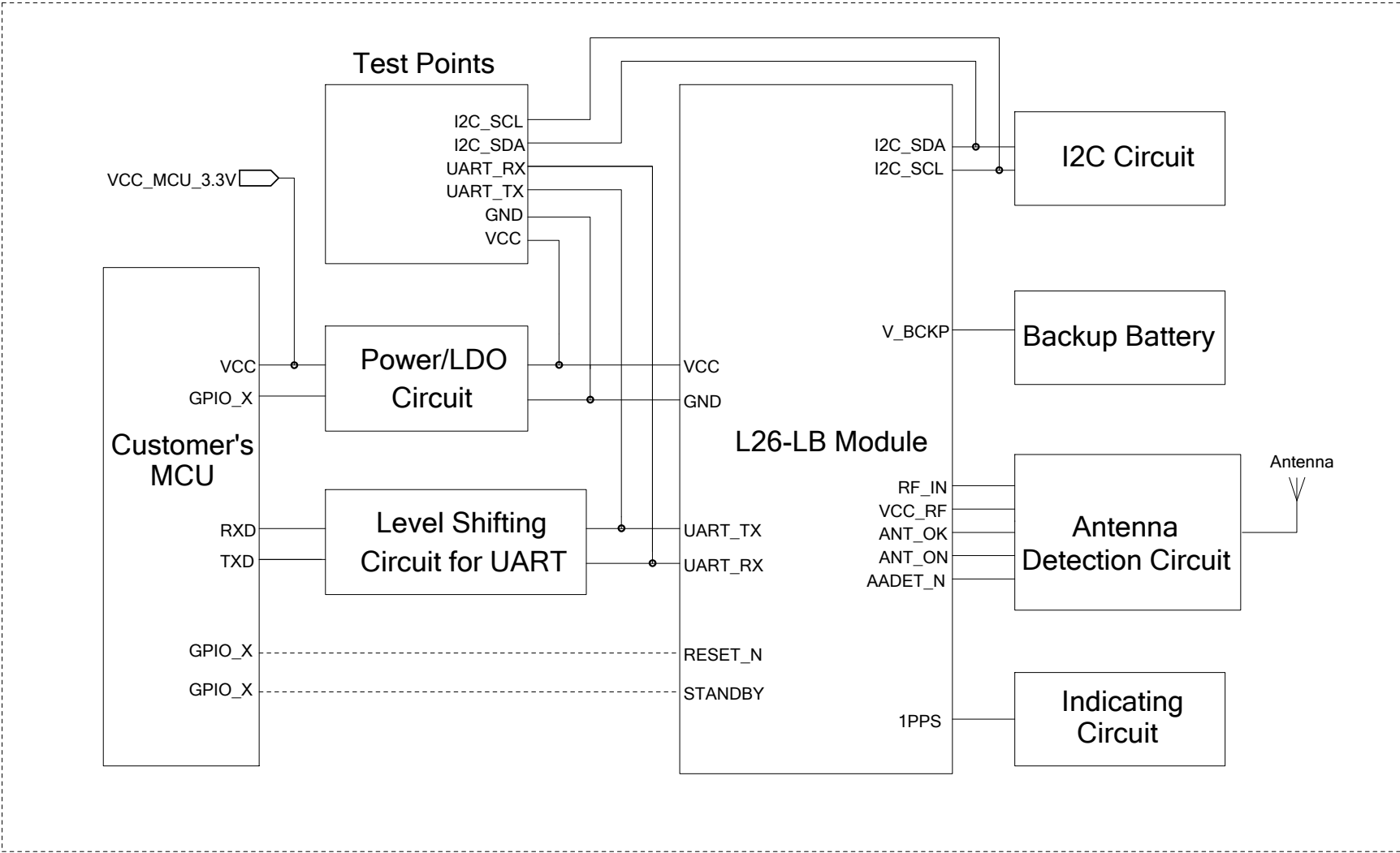# Contents

1 Reference Design

1.1. Introduction

This document provides the reference design of Quectel L26-LB GNSS module, including the design of power supply, UART and antenna interfaces.

1.2. Schematics

The schematics illustrated in the following pages are provided for your reference only.
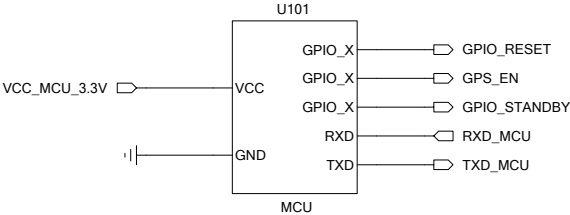
Block Diagram

Test Points

- I2C_SCL
- I2C_SDA
- UART_RX
- UART_TX
- GND
- VCC

VCC_MCU_3.3V

Customer's MCU
- VCC
- GPIO_X
- RXD
- TXD
- GPIO_X
- GPIO_X

Power/LDO Circuit

Level Shifting Circuit for UART

L26-LB Module
- VCC
- GND
- UART_TX
- UART_RX
- RESET_N
- STANDBY
- I2C_SDA
- I2C_SCL
- V_BCKP
- RF_IN
- VCC_RF
- ANT_OK
- ANT_ON
- AADET_N
- 1PPS

I2C Circuit

Backup Battery

Antenna Detection Circuit

Antenna

Indicating Circuit

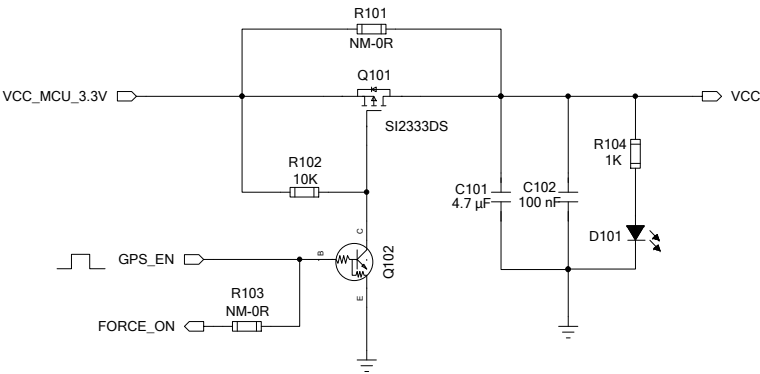|		
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3.3V Power Suppply and UART Circuits

Customer's MCU

U101

VCC_MCU_3.3V	→ VCC	GPIO_X	GPIO_RESET
		GPIO_X	GPS_EN
		GPIO_X	GPIO_STANDBY
		RXD	RXD_MCU
	GND	TXD	TXD_MCU

MCU

Power Management Circuit (Optional)

R101
NM-0R

Q101
SI2333DS

VCC_MCU_3.3V → VCC

R102
10K

R104
1K

C101
4.7 µF
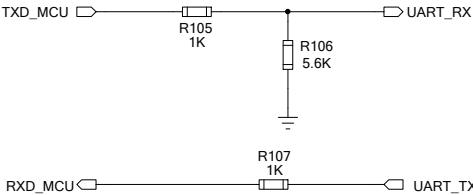
C102
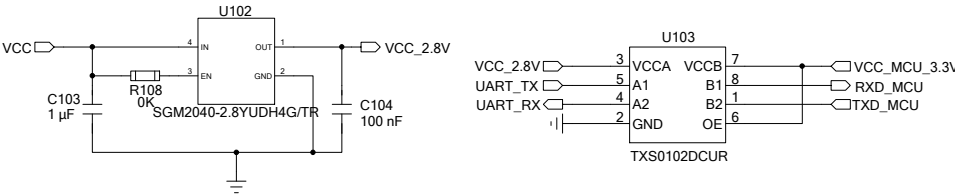100 nF

D101

GPS_EN

Q102

R103
NM-0R

FORCE_ON

Note:

There are two ways to enter/exit backup mode:

1. Sending $PMTK225,4*2F command makes the module enter backup mode. In such a case, the only way to wake up the module is by pulling FORCE_ON high. In the solution, Q101, Q102 and R102 are not mounted; R101 and R103 are 0 Ω.

2. Cutting off the power supply of VCC while keeping V_BCKP powered, the module will enter backup mode. As soon as the VCC power supply is restored, the module enters full on mode immediately. In the solution, Q101, Q102 and R102 are mounted; R101 and R103 are not mounted.

Level Shifting for UART - Resistor Solution

TXD_MCU → R105 1K → UART_RX

R106
5.6K

R107
1K

RXD_MCU → UART_TX

Level Shifting for UART - Level Shifter IC Solution

U102

| VCC | 4 IN | OUT 1 | VCC_2.8V |
| | 3 EN | GND 2 | |

C103
1 µF

R108
0K

SGM2040-2.8YUDH4G/TR

C104
100 nF

U103

VCC_2.8V	3 VCCA	VCCB 7	VCC_MCU_3.3V
UART_TX	5 A1	B1 8	RXD_MCU
UART_RX	4 A2	B2 1	TXD_MCU
	2 GND	OE 6	

TXS0102DCUR

Notes:

1. The above level shifting circuits realize the voltage-level shifting between VCC_MCU_3.3V and 2.8 V (power domain of UART), and block the leakage current from the power-on devices to power-off devices.

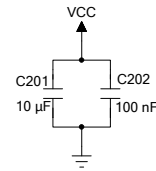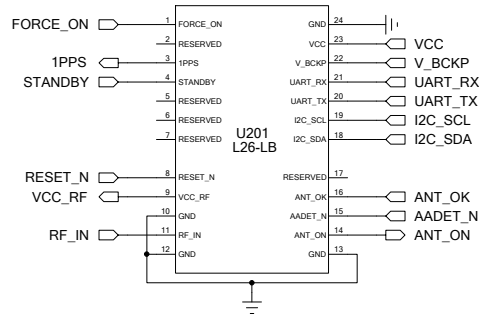2. The level shifter IC solution generally requires VCCA ≤ VCCB, please pay attention to the voltage relationship.

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Module Interfaces

Module Interfaces

U201
L26-LB

Pin	Signal
1	FORCE_ON
2	RESERVED
3	1PPS
4	STANDBY
5	RESERVED
6	RESERVED
7	RESERVED
8	RESET_N
9	VCC_RF
10	GND
11	RF_IN
12	GND
24	GND
23	VCC
22	V_BCKP
21	UART_RX
20	UART_TX
19	I2C_SCL
18	I2C_SDA
17	RESERVED
16	ANT_OK
15	AADET_N
14	ANT_ON
13	GND

FORCE_ON
1PPS
STANDBY
RESET_N
VCC_RF
RF_IN

VCC
V_BCKP
UART_RX
UART_TX
I2C_SCL
I2C_SDA
ANT_OK
AADET_N
ANT_ON

VCC

C201 10 µF
C202 100 nF

Test Points

L26_LB_SDA	I2C_SDA
L26_LB_SCL	I2C_SCL
L26_LB_TXD	UART_TX
L26_LB_RXD	UART_RX
L26_LB_VCC	VCC
GND	GND

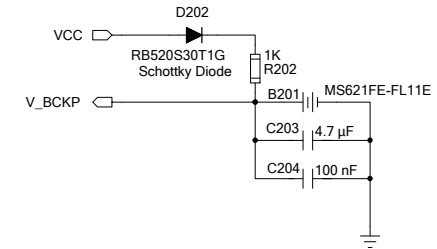**Notes:**

1. UART can be used used for NMEA sentences output and firmware upgrade.

2. When I2C interface is supported, I2C interface will be used for NMEA sentences output by default.
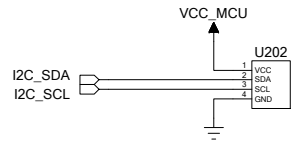
RTC Backup Power Supply

D202
RB520S30T1G
Schottky Diode

VCC

1K R202

B201 MS621FE-FL11E

V_BCKP

C203 4.7 µF

C204 100 nF

Note:

V_BCKP is designed to supply power for L26-LB RTC logic circuit when VCC is powered off.

I2C Circuit

VCC_MCU

U202

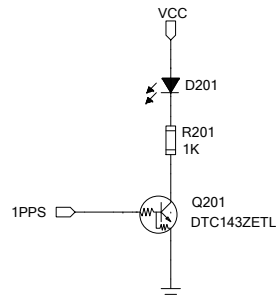| Pin	Signal
1	VCC
2	SDA
3	SCL
4	GND

I2C_SDA
I2C_SCL

Notes:

1. I2C_SDA/I2C_SCL is pulled up to 2.8 V inside the module.

2. The power domain of I2C is 2.8 V. If the system voltage is not consistent with it, a level shifter circuit must be used.
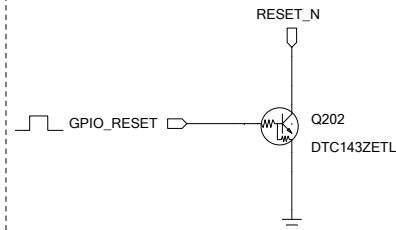
Indicating Circuit

VCC

D201

R201 1K

Q201 DTC143ZETL

1PPS

Note:

The 1PPS indicator will blink at 1 Hz frequency after fixing the position.

Reset Circuit

RESET_N

GPIO_RESET

Q202 DTC143ZETL

Note:

RESET_N has been pulled up internally.

Standby Circuit

STANDBY

GPIO_STANDBY

Q203 DTC143ZETL
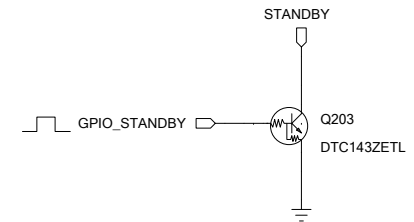
Notes:

1. STANDBY has been pulled up internally.

2. Enter standby mode: change the STANDBY pin from high to low level.

3. Exit standby mode: change the STANDBY pin from low to high level. For more details, please refer to *Quectel_L26-LB_Hardware_Design*.
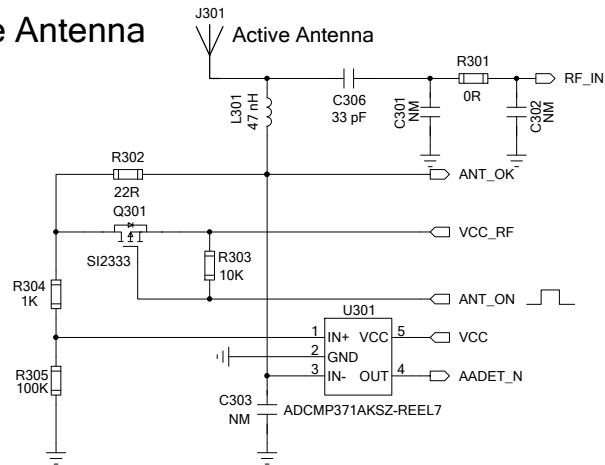
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Antenna Interface

Active Antenna

J301 Active Antenna
L301 47 nH
C306 33 pF
C301 NM
R301 0R
C302 NM
RF_IN
ANT_OK
R302 22R
Q301
SI2333
R303 10K
VCC_RF
R304 1K
ANT_ON
R305 100K
U301
1 IN+ VCC 5
2 GND
3 IN- OUT 4
C303 NM
ADCMP371AKSZ-REEL7
VCC
AADET_N

Notes:

1. The comparator U301 is used to distinguish the antenna connection status, either normal or open circuit.
   When ANT_ON is pulled down, the voltage division circuit (R304, R305) divides the voltage of VCC_RF.
   It is recommended to adjust the value of R304 and R305 appropriately according to the power consumption of
   active antenna, so as to achieve the following conditions:
   When antenna status is open circuit: pin 4 (output) of U301 at low level
   When antenna status is normal: pin 4 (output) of U301 at high level

2. The R_BIAS (R302) is a must, otherwise the module may be damaged permanently when the antenna
   is short circuited.

3. VCC_RF can be used to supply power for the active antenna. Its voltage range is 2.8 to 4.3 V (VCC_RF = VCC),
   and the typical value is 3.3 V. If VCC_RF cannot meet the antenna's power supply requirements,
   an external LDO is needed.

4. Please keep 50 Ω impedance for RF traces, and keep the trace length as short as possible.
   For more details, please refer to *Quectel_L26-LB_Hardware_Design*.

Passive Antenna

J302
R306 0R
RF_IN
C304 NM
C305 NM
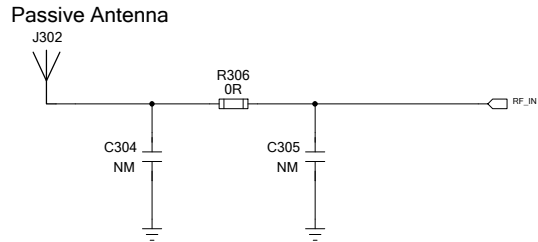
Notes:

1. The Π type matching circuit (R306, C304, C305) is reserved for antenna impedance matching.
   By default, C304 and C305 are not mounted and R306 is 0 Ω.

2. Please keep 50 Ω impedance for RF traces, and keep the trace length as short as possible.
   For more details, please refer to *Quectel_L26-LB_Hardware_Design*.