

# EG95 Series

# Hardware Design

**LTE Standard Module Series**

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## Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any cellular terminal or mobile incorporating the module. Manufacturers of the cellular terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for customers' failure to comply with these precautions.



Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.



Switch off the cellular terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.



Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.



Cellular terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergency help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the cellular terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.



The cellular terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.



In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other cellular terminals. Areas with explosive or potentially explosive atmospheres include fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.

# About the Document

## Revision History

Version	Date	Author	Description
1.0	2017-03-22	Felix YIN/ Yeoman CHEN/ Jackie WANG	Initial
1.1	2018-01-04	Yeoman CHEN/ Rex WANG	<ol style="list-style-type: none"> <li>1. Added band B28A.</li> <li>2. Updated the description of UMTS and GSM features in Table 2.</li> <li>3. Updated the functional diagram in Figure 1.</li> <li>4. Updated module operating frequencies in Table 21.</li> <li>5. Updated current consumption in Table 26.</li> <li>6. Updated the conducted RF receiving sensitivity in Table 28.</li> <li>7. Updated the GPRS multi-slot classes in Table 33.</li> <li>8. Added thermal consideration in Chapter 5.8</li> <li>9. Added a GND pad in each of the four corners of the module's footprint in Chapter 6.2.</li> <li>10. Added packaging information in Chapter 7.3.</li> </ol>
1.2	2018-03-14	Felix YIN/ Rex WANG	<ol style="list-style-type: none"> <li>1. Added the description of EG95-NA.</li> <li>2. Updated the functional diagram in Figure 1.</li> <li>3. Updated pin assignment in Figure 2.</li> <li>4. Updated GNSS function in Table 1.</li> <li>5. Updated GNSS Features in Table 2.</li> <li>6. Updated reference circuit of USB interface in Figure 21.</li> <li>7. Added description of GNSS receiver in Chapter 4.</li> <li>8. Updated pin definition of RF antenna in</li> </ol>

			<ul style="list-style-type: none"> <li>Table 21.</li> <li>9. Updated module operating frequencies in Table 22.</li> <li>10. Added description of GNSS antenna interface in Chapter 5.2.</li> <li>11. Updated antenna requirements in Table 25.</li> <li>12. Updated RF output power in Table 32.</li> </ul>
1.3	2019-05-24	Ward WANG/ Nathan LIU/ Rex WANG	<ul style="list-style-type: none"> <li>1. Added variant EG95-EX and related information.</li> <li>2. Updated functional diagram in Figure 1.</li> <li>3. Updated pin assignment (top view) in Figure 2.</li> <li>4. Updated pin description in Table 4.</li> <li>5. Updated star structure of power supply in Figure 8.</li> <li>6. Updated the reference circuit of turning on the module using PWRKEY in Figure 10.</li> <li>7. Updated the power-on scenario in Figure 12.</li> <li>8. Updated reference circuit of SPI interface with peripherals in Figure 25.</li> <li>9. Updated GNSS performance in Table 20.</li> <li>10. Updated module operating frequencies in Table 22.</li> <li>11. Updated GNSS frequency in Table 24.</li> <li>12. Updated antenna requirements in Table 25.</li> <li>13. Updated EG95-NA current consumption in Table 30.</li> <li>14. Added EG95-EX current consumption in Table 31.</li> <li>15. Updated EG95-E conducted RF receiving sensitivity in Table 34.</li> <li>16. Updated EG95-NA conducted RF receiving sensitivity in Table 35.</li> <li>17. Added EG95-EX conducted RF receiving sensitivity in Table 36.Updated GNSS current consumption of EG95 in Table 32.Updated related documents in Table 38.Updated reference circuit of PWRKEY interface in Figure 10.</li> <li>18. Updated description of (U)SIM in Chapter 3.9.</li> <li>19. Updated description of UART in Chapter 3.11.</li> </ul>

			<ul style="list-style-type: none"> <li>20. Added description of ADC interface in Chapter 3.16.</li> <li>21. Added description of USB_BOOT interface in Chapter 3.18.</li> <li>22. Updated description of manufacturing and soldering in Chapter 8.2.</li> </ul>
1.4	2019-07-05	Ward WANG	<ul style="list-style-type: none"> <li>1. Updated supported protocols (Table 2).</li> <li>2. Updated timing of turning on module (Figure 12).</li> <li>3. DFOTA is developed.</li> <li>4. Updated description of USB_BOOT interface and timing sequence for entering emergency download mode (Chapter 3.18 and Figure 29).</li> </ul>
1.5	2019-08-09	Fanny CHEN/ Rex WANG	<ul style="list-style-type: none"> <li>1. Added ThreadX module EG95-NAX and updated related contents (Table 1 and 4, Chapter 2.2, 2.3, 3.2 and 5).</li> <li>2. Updated module operating frequencies (Table 25).</li> <li>3. Updated antenna requirements (Table 28).</li> <li>4. Added current consumption of EG95-NAX (Table 35).</li> <li>5. Updated RF output power (Table 37).</li> <li>6. Updated EG95-NA conducted RF receiving sensitivity (Table 39).</li> <li>7. Added EG95-NAX conducted RF receiving sensitivity (Table 41).</li> </ul>
1.6	2019-11-07	Ward WANG	<ul style="list-style-type: none"> <li>1. Removed related information of ThreadX OS.</li> <li>2. Updated the supported USB serial drivers (Table 2)</li> <li>3. Updated the notes for GNSS performance (Chapter 4.2).</li> <li>4. Updated the AT command be used to disable the receive diversity (Chapter 5.1.3).</li> </ul>
1.7	2020-04-15	Ward WANG	<ul style="list-style-type: none"> <li>1. Updated description of airplane mode (Chapter 3.5.2).</li> <li>2. Updated the functions of main UART interface (Chapter 3.11).</li> <li>3. Added the note about the standard that the package warpage level of the module conforms to (Chapter 7.1).</li> <li>4. Updated module storage information (Chapter 8.1).</li> </ul>

			<ol style="list-style-type: none"> <li>5. Updated module manufacturing and soldering information (Chapter 8.2).</li> </ol>
1.8	2020-10-21	Power JIN/ Frank WANG	<ol style="list-style-type: none"> <li>1. Added EG95-AUX and related information (Table 1, 37 and 45).</li> <li>2. Added EG95-NAXD and related information (Table 1, 36 and 44).</li> <li>3. Updated the AT command for the operation of ANT_MAIN and ANT_DIV (Chapter 5.1.3).</li> <li>4. Added EG95-NA/-EX/-NAX/-NAXD/-AUX bottom dimensions (Figure 43).</li> <li>5. Updated top view of the module (Figure 45).</li> <li>6. Added EG95-NA/-EX/-NAX/-NAXD/-AUX bottom view (Figure 47).</li> <li>7. Added a note to clarify the precautions if a conformal coating is necessary for the module (Chapter 8.2).</li> </ol>
1.9	2022-05-07	Joe MA/ Frank WANG	<ol style="list-style-type: none"> <li>1. Updated the module size information (Chapter 2.1 &amp; Table 3 &amp; Chapter 6.1).</li> <li>2. Updated the USB serial drivers and the module weight (Table 3).</li> <li>3. Updated the recommended footprint, and the top and bottom views of the module (Chapter 6.2 &amp; 6.3).</li> <li>4. Updated the description of storage conditions (Chapter 7.1)</li> <li>5. Updated the information of the manufacturing and soldering (Chapter 7.2).</li> <li>6. Updated the note description of label, conformal coating, ultrasonic cleaning and soldering (Chapter 7.2).</li> <li>7. Updated the packaging specifications (Chapter 7.3).</li> </ol>



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# 1 Introduction

This document defines EG95 series module, and describes its air interface and hardware interfaces which are connected with your applications.

This document can help you quickly understand module interface specifications, electrical and mechanical details, as well as other related information of EG95 series module. With application note and user guide, you can use EG95 series module to design and set up mobile applications easily.

## 1.1. Special Mark

**Table 1: Special Mark**

Mark	Definition
*	Unless otherwise specified, when an asterisk (*) is used after a function, feature, interface, pin name, AT command, or argument, it indicates that the function, feature, interface, pin, AT command, or argument is under development and currently not supported; and the asterisk (*) after a model indicates that the sample of the model is currently unavailable.

## 2 Product Overview

### 2.1. Frequency Bands and Functions

EG95 series module is an embedded 4G wireless communication module with receive diversity. It supports LTE/WCDMA/GSM wireless communication, and provides data connectivity on LTE-FDD, DC-HSDPA, HSPA+, HSDPA, HSUPA, WCDMA, EDGE and GPRS networks. It can also provide voice functionality <sup>1</sup> to meet your specific application demands.

The following table shows the frequency bands of EG95 series module.

**Table 2: Frequency Bands and GNSS Functions of EG95 Series Module**

Module	LTE Bands (with Rx-diversity)	WCDMA (with Rx-diversity)	GSM	GNSS <sup>2</sup>
EG95-E	FDD: B1/B3/B7/B8/B20/B28A	B1/B8	EGSM900/ DCS1800/	-
EG95-NA	FDD: B2/B4/B5/B12/B13	B2/B4/B5	-	
EG95-EX	FDD: B1/B3/B7/B8/B20/B28	B1/B8	EGSM900/ DCS1800/	
EG95-NAX	FDD: B2/B4/B5/B12/B13/B25/B26	B2/B4/B5	-	GPS, GLONASS, BDS, Galileo, QZSS
EG95-NAXD	FDD: B2/B4/B5/B12/B13/B25/B26	B2/B4/B5	-	
EG95-AUX	FDD: B1/B2/B3/B4/B5/B7/B8 B28/B66	B1/B2/B5/B8	GSM850/ EGSM900/ DCS1800/ PCS1900	

With a compact profile of 29.0 mm × 25.0 mm × 2.3 mm (EG95-E), or 29.0 mm × 25.0 mm × 2.45 mm (EG95-NA/-EX/-NAX/-NAXD/-AUX), EG95 series can meet almost all requirements for M2M applications such as automation, smart metering, tracking system, security, router, wireless POS, mobile computing device, PDA phone, tablet PC, etc.

<sup>1</sup> EG95 series contains **Data + Voice** version and **Data-only** version.

<sup>2</sup> GNSS function is optional.



EG95 series module is an SMD type module which can be embedded into applications through its 106 LGA pins. EG95 series module is integrated with internet service protocols like TCP, UDP and PPP. Extended AT commands have been developed for you to use these internet service protocols easily.

## 2.2. Key Features

The following table describes the detailed features of EG95 series module.

**Table 3: Key Features of EG95 Series Module**

Features	Description
Power Supply	<ul style="list-style-type: none"> <li>● Supply voltage: 3.3–4.3 V</li> <li>● Typical supply voltage: 3.8 V</li> </ul>
Transmitting Power	<ul style="list-style-type: none"> <li>● Class 4 (33 dBm <math>\pm</math>2 dB) for GSM850</li> <li>● Class 4 (33 dBm <math>\pm</math>2 dB) for EGSM900</li> <li>● Class 1 (30 dBm <math>\pm</math>2 dB) for DCS1800</li> <li>● Class 1 (30 dBm <math>\pm</math>2 dB) for PCS1900</li> <li>● Class E2 (27 dBm <math>\pm</math>3 dB) for GSM850 8-PSK</li> <li>● Class E2 (27 dBm <math>\pm</math>3 dB) for EGSM900 8-PSK</li> <li>● Class E2 (26 dBm <math>\pm</math>3 dB) for DCS1800 8-PSK</li> <li>● Class E2 (26 dBm <math>\pm</math>3 dB) for PCS1900 8-PSK</li> <li>● Class 3 (24 dBm +1/-3 dB) for WCDMA bands</li> <li>● Class 3 (23 dBm <math>\pm</math>2 dB) for LTE-FDD bands</li> </ul>
LTE Features	<ul style="list-style-type: none"> <li>● Support up to non-CA Cat 4 FDD</li> <li>● Support 1.4/3/5/10/15/20 MHz RF bandwidth</li> <li>● Support MIMO in DL direction</li> <li>● FDD: Max. 150 Mbps (DL)/Max. 50 Mbps (UL)</li> </ul>
UMTS Features	<ul style="list-style-type: none"> <li>● Support 3GPP Rel-8 DC-HSDPA, HSPA+, HSDPA, HSUPA and WCDMA</li> <li>● Support QPSK, 16QAM and 64QAM modulation</li> <li>● DC-HSDPA: Max. 42 Mbps (DL)</li> <li>● HSUPA: Max. 5.76 Mbps (UL)</li> <li>● WCDMA: Max. 384 kbps (DL)/ Max. 384 kbps (UL)</li> </ul>
GSM Features	<ul style="list-style-type: none"> <li>● <b>R99:</b> CSD: 9.6 kbps</li> <li>● <b>GPRS:</b> Support GPRS multi-slot class 33 (33 by default) Coding scheme: CS-1, CS-2, CS-3 and CS-4 Max. 107 kbps (DL), Max. 85.6 kbps (UL)</li> <li>● <b>EDGE:</b></li> </ul>

	<p>Support EDGE multi-slot class 33 (33 by default)</p> <p>Support GMSK and 8-PSK for different MCS (Modulation and Coding Scheme)</p> <p>Downlink coding schemes: MCS 1–9</p> <p>Uplink coding schemes: MCS 1–9</p> <p>Max. 296 kbps (DL)/Max. 236.8 kbps (UL)</p>
Internet Protocol Features	<ul style="list-style-type: none"> <li>● Support TCP/UDP/PPP/FTP/FTPS/HTTP/HTTPS/NTP/PING/QMI/NITZ/MMS/SMTP/SSL/MQTT/FILE/CMUX/SMTPS protocols</li> <li>● Support PAP and CHAP protocols for PPP connections</li> </ul>
SMS	<ul style="list-style-type: none"> <li>● Text and PDU modes</li> <li>● Point-to-point MO and MT</li> <li>● SMS cell broadcast</li> <li>● SMS storage: ME by default</li> </ul>
(U)SIM Interfaces	<ul style="list-style-type: none"> <li>● Support 1.8 V and 3.0 V (U)SIM cards</li> </ul>
Audio Features	<ul style="list-style-type: none"> <li>● Support one digital audio interface: PCM interface</li> <li>● GSM: HR/FR/EFR/AMR/AMR-WB</li> <li>● WCDMA: AMR/AMR-WB</li> <li>● LTE: AMR/AMR-WB</li> <li>● Support echo cancellation and noise suppression</li> </ul>
PCM Interface	<ul style="list-style-type: none"> <li>● Used for audio function with external codec</li> <li>● Support 16-bit linear data format</li> <li>● Support long frame synchronization and short frame synchronization</li> <li>● Support master and slave modes, but must be the master in long frame synchronization</li> </ul>
USB Interface	<ul style="list-style-type: none"> <li>● Compliant with USB 2.0 specification (slave only); the data transfer rate can reach up to 480 Mbps</li> <li>● Used for AT command communication, data transmission, GNSS NMEA sentences output, software debugging, firmware upgrade and voice over USB</li> <li>● Support USB serial drivers for: Windows 7/8/8.1/10/11, Linux 2.6–5.15, Android 4.x–12.x, etc.</li> </ul>
UART Interface	<ul style="list-style-type: none"> <li>● <b>Main UART:</b> Used for AT command communication and data transmission Baud rates reach up to 921600 bps, 115200 bps by default Supports RTS and CTS hardware flow control</li> <li>● <b>Debug UART:</b> Used for Linux console and log output 115200 bps baud rate</li> </ul>
SPI Interface	<ul style="list-style-type: none"> <li>● Provides a duplex, synchronous and serial communication link with the peripheral devices.</li> <li>● Dedicated to one-to-one connection, without chip selection.</li> <li>● 1.8 V operation voltage with clock rates up to 50 MHz.</li> </ul>

Rx-diversity	<ul style="list-style-type: none"> <li>● Support LTE/WCDMA Rx-diversity</li> </ul>
GNSS Features	<ul style="list-style-type: none"> <li>● Protocol: NMEA 0183</li> <li>● Data update rate: 1 Hz by default</li> </ul>
AT Commands	<ul style="list-style-type: none"> <li>● Compliant with <i>3GPP TS 27.007</i>, <i>3GPP TS 27.005</i></li> <li>● Quectel enhanced AT commands</li> </ul>
Network Indication	<ul style="list-style-type: none"> <li>● NETLIGHT pin for network activity status indication</li> </ul>
Antenna Interfaces	<ul style="list-style-type: none"> <li>● Main antenna interface (ANT_MAIN)</li> <li>● Rx-diversity antenna interface (ANT_DIV)</li> <li>● GNSS antenna interface (ANT_GNSS) <sup>3</sup></li> </ul>
Physical Characteristics	<ul style="list-style-type: none"> <li>● Size: (29.0 ±0.15) mm × (25.0 ±0.15) mm × (2.3 ±0.2) mm (EG95-E) (29.0 ±0.15) mm × (25.0 ±0.15) mm × (2.45 ±0.2) mm (EG95-NA/-EX/-NAX/-NAXD/-AUX)</li> <li>● Package: LGA</li> <li>● Weight: approx. 4.1 g (EG95-E) approx. 4.2 g (EG95-NA/-EX/-NAX/-NAXD/-AUX)</li> </ul>
Temperature Range	<ul style="list-style-type: none"> <li>● Operating temperature range: -35 °C to +75 °C <sup>4</sup></li> <li>● Extended temperature range: -40 °C to +85 °C <sup>5</sup></li> <li>● Storage temperature range: -40 °C to +90 °C</li> </ul>
Firmware Upgrade	<ul style="list-style-type: none"> <li>● USB interface or DFOTA</li> </ul>
RoHS	<ul style="list-style-type: none"> <li>● All hardware components are fully compliant with EU RoHS directive</li> </ul>

## 2.3. Functional Diagram

The following figure shows a block diagram of EG95 series and illustrates the major functional parts.

- Power management
- Baseband
- DDR + NAND flash
- Radio frequency
- Peripheral interfaces

<sup>3</sup> GNSS antenna interface is only supported on EG95-NA/-EX/-NAX/-NAXD/-AUX.

<sup>4</sup> Within the operating temperature range, the module meets 3GPP specifications.

<sup>5</sup> Within the extended temperature range, the module remains the ability to establish and maintain functions such as voice, SMS, data transmission, etc., without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as  $P_{out}$ , may exceed the specified tolerances of 3GPP. When the temperature returns to the operating temperature range, the module meets 3GPP specifications again.

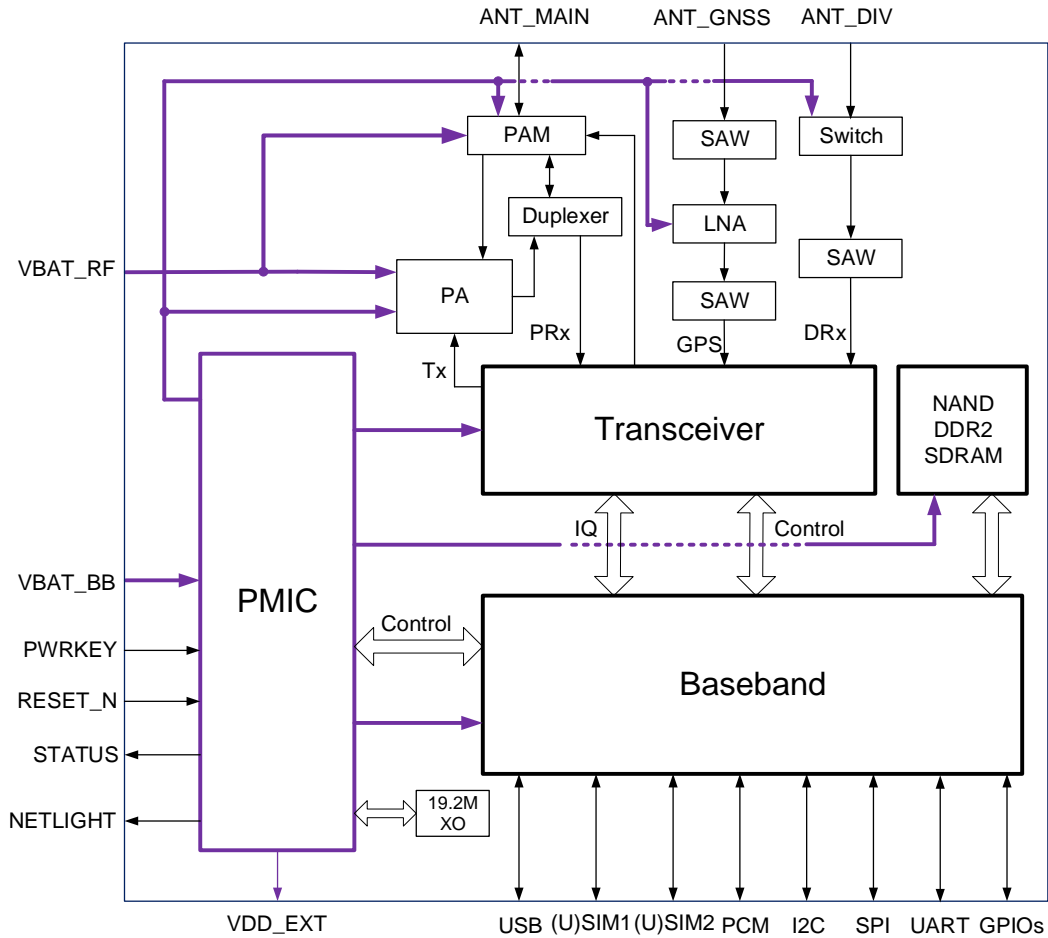


Figure 1: Functional Diagram <sup>6</sup>

## 2.4. EVB Kit

To facilitate application design with the module, Quectel supplies an evaluation board (UMTS&LTE EVB), USB to RS-232 converter cable, earphone, antenna and other peripherals to control or test the module. For more details, see **document [1]**.

<sup>6</sup> GNSS antenna interface is only supported on EG95-NA/-EX/-NAX/-NAXD/-AUX.

# 3 Application Interfaces

## 3.1. General Description

EG95 series is equipped with 106 LGA pins that can be connected to cellular application platform. The subsequent chapters will provide detailed descriptions of the following functions/interfaces.

- Power supply
- (U)SIM interfaces
- USB interface
- UART interfaces
- PCM and I2C interfaces
- SPI interface
- Indication signals
- ADC interface
- USB\_BOOT interface

### 3.2. Pin Assignment

The following figure shows the pin assignment of EG95 series module.

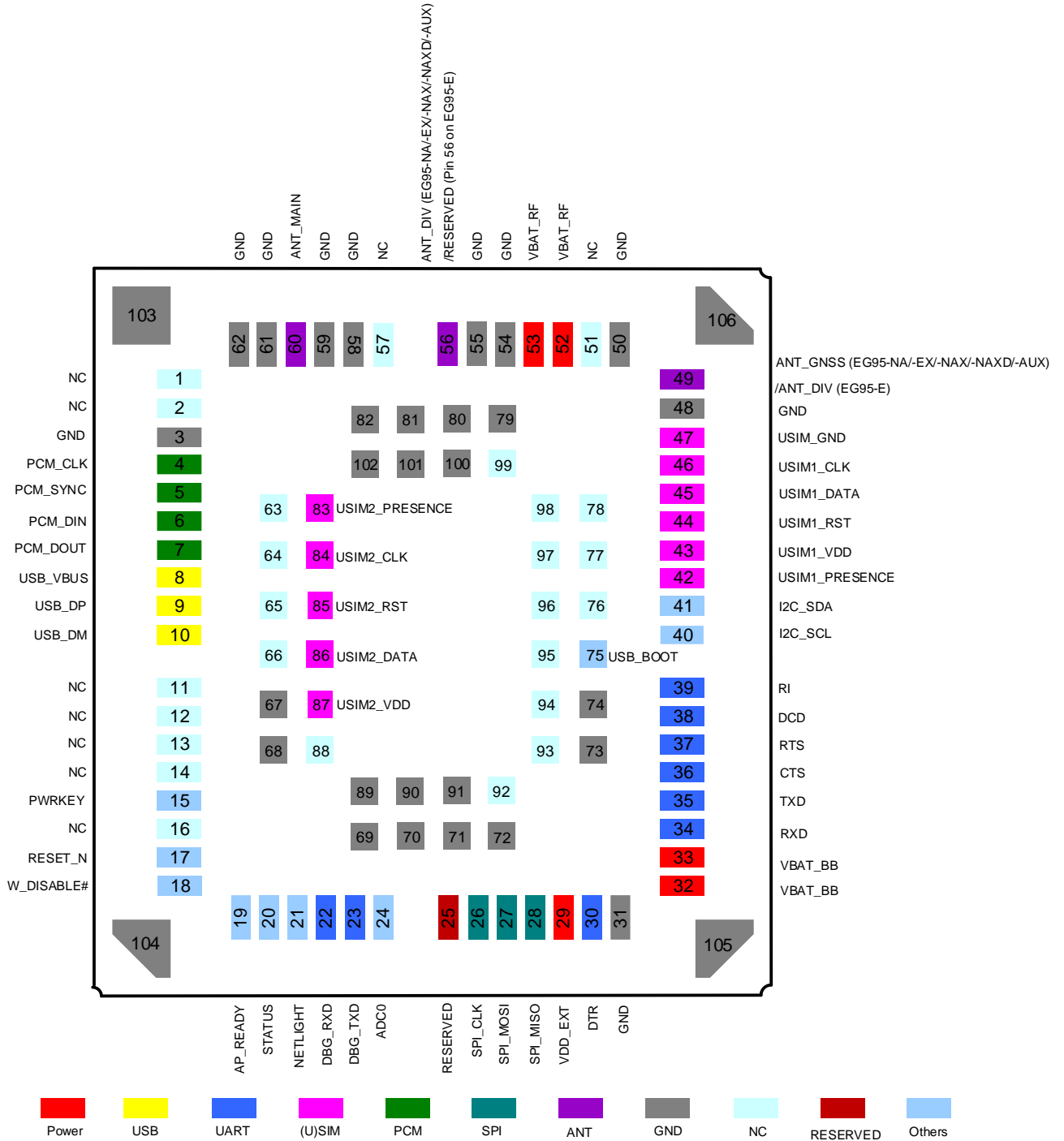


Figure 2: Pin Assignment (Top View)

**NOTE**

1. PWRKEY output voltage is 0.8 V because of the diode drop in the baseband chipset.
2. Keep all RESERVED pins and unused pins unconnected.
3. GND pins should be connected to ground in the design.
4. Please note that the definition of pin 49 and pin 56 is different among EG95-E and EG95-NA/-EX/-NAX/-NAXD/-AUX. For more details, see **Table 5**.

### 3.3. Pin Description

The following tables show the pin definition of EG95 series module.

**Table 4: Definition of I/O Parameters**

Type	Description
AI	Analog Input
AO	Analog Output
AIO	Analog Input/Output
DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output
OD	Open Drain
PI	Power Input
PO	Power Output

**Table 5: Pin Description**

Power Supply					
Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
VBAT_BB	32, 33	PI	Power supply for module's baseband	Vmax = 4.3 V Vmin = 3.3 V	It must be provided with sufficient current up to

			part	Vnom = 3.8 V	0.8 A.
VBAT_RF	52, 53	PI	Power supply for module's RF part	Vmax = 4.3 V Vmin = 3.3 V Vnom = 3.8 V	It must be provided with sufficient current up to 1.8 A in a burst transmission.
VDD_EXT	29	PO	Provide 1.8 V for external circuit	Vnorm = 1.8 V I <sub>o</sub> max = 50 mA	Power supply for external GPIO's pull up circuits. If unused, keep it open.
GND	3, 31, 48, 50, 54, 55, 58, 59, 61, 62, 67–74, 79–82, 89–91, 100–106				

**Power-on/off**

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
PWRKEY	15	DI	Turn on/off the module		The output voltage is 0.8 V because of the diode drop in the baseband chipset.
RESET_N	17	DI	Reset the module	V <sub>IH</sub> max = 2.1 V V <sub>IH</sub> min = 1.3 V V <sub>IL</sub> max = 0.5 V	Pull-up to 1.8 V internally. Active LOW. If unused, keep it open.

**Status Indication**

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
STATUS	20	DO	Indicate the module's operating status	V <sub>OH</sub> min = 1.35 V V <sub>OL</sub> max = 0.45 V	1.8 V power domain. If unused, keep these pins open.
NETLIGHT	21	DO	Indicate the module's network activity status		

**USB Interface**

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
USB_VBUS	8	PI	USB connection detect	Vmax = 5.25 V Vmin = 3.0 V Vnom = 5.0 V	Typical: 5.0 V If unused, keep it open.
USB_DP	9	AIO	USB differential data (+)		USB 2.0 compliant. Require differential



					impedance of 90 Ω.
USB_DM	10	AIO	USB differential data (-)		USB 2.0 compliant. Require differential impedance of 90 Ω.

**(U)SIM Interfaces**

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
USIM_GND	47		Specified ground for (U)SIM card		Connect to ground of (U)SIM card connector.
USIM1_VDD	43	PO	(U)SIM1 card power supply	$I_{Omax} = 50 \text{ mA}$  <b>For 1.8 V (U)SIM:</b> $V_{max} = 1.9 \text{ V}$ $V_{min} = 1.7 \text{ V}$  <b>For 3.0 V (U)SIM:</b> $V_{max} = 3.05 \text{ V}$ $V_{min} = 2.7 \text{ V}$	Either 1.8 V or 3.0 V is supported by the module automatically.
USIM1_DATA	45	DIO	(U)SIM1 card data	<b>For 1.8 V (U)SIM:</b> $V_{ILmax} = 0.6 \text{ V}$ $V_{IHmin} = 1.2 \text{ V}$ $V_{OLmax} = 0.45 \text{ V}$ $V_{OHmin} = 1.35 \text{ V}$  <b>For 3.0 V (U)SIM:</b> $V_{ILmax} = 1.0 \text{ V}$ $V_{IHmin} = 1.95 \text{ V}$ $V_{OLmax} = 0.45 \text{ V}$ $V_{OHmin} = 2.55 \text{ V}$	
USIM1_CLK	46	DO	(U)SIM1 card clock	<b>For 1.8 V (U)SIM:</b> $V_{OLmax} = 0.45 \text{ V}$ $V_{OHmin} = 1.35 \text{ V}$	
USIM1_RST	44	DO	(U)SIM1 card reset	<b>For 3.0 V (U)SIM:</b> $V_{OLmax} = 0.45 \text{ V}$ $V_{OHmin} = 2.55 \text{ V}$	
USIM1_PRESENCE	42	DI	(U)SIM1 card hot plug detection	$V_{ILmin} = -0.3 \text{ V}$ $V_{ILmax} = 0.6 \text{ V}$ $V_{IHmin} = 1.2 \text{ V}$ $V_{IHmax} = 2.0 \text{ V}$	1.8 V power domain. If unused, keep it open.

USIM2_VDD	87	PO	(U)SIM2 card power supply	<p><b>For 1.8 V (U)SIM:</b>  <math>V_{max} = 1.9\text{ V}</math>  <math>V_{min} = 1.7\text{ V}</math></p> <p><b>For 3.0 V (U)SIM:</b>  <math>V_{max} = 3.05\text{ V}</math>  <math>V_{min} = 2.7\text{ V}</math>  <math>I_{Omax} = 50\text{ mA}</math></p>	Either 1.8 V or 3.0 V is supported by the module automatically.
USIM2_DATA	86	DIO	(U)SIM2 card data	<p><b>For 1.8 V (U)SIM:</b>  <math>V_{ILmax} = 0.6\text{ V}</math>  <math>V_{IHmin} = 1.2\text{ V}</math>  <math>V_{OLmax} = 0.45\text{ V}</math>  <math>V_{OHmin} = 1.35\text{ V}</math></p> <p><b>For 3.0 V (U)SIM:</b>  <math>V_{ILmax} = 1.0\text{ V}</math>  <math>V_{IHmin} = 1.95\text{ V}</math>  <math>V_{OLmax} = 0.45\text{ V}</math>  <math>V_{OHmin} = 2.55\text{ V}</math></p>	
USIM2_CLK	84	DO	(U)SIM2 card clock	<p><b>For 1.8 V (U)SIM:</b>  <math>V_{OLmax} = 0.45\text{ V}</math>  <math>V_{OHmin} = 1.35\text{ V}</math></p>	
USIM2_RST	85	DO	(U)SIM2 card reset	<p><b>For 3.0 V (U)SIM:</b>  <math>V_{OLmax} = 0.45\text{ V}</math>  <math>V_{OHmin} = 2.55\text{ V}</math></p>	
USIM2_PRESENCE	83	DI	(U)SIM2 card hot plug detection	$V_{ILmin} = -0.3\text{ V}$ $V_{ILmax} = 0.6\text{ V}$ $V_{IHmin} = 1.2\text{ V}$ $V_{IHmax} = 2.0\text{ V}$	1.8 V power domain. If unused, keep it open.

**Main UART Interface**

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
RI	39	DO	Ring indication	$V_{OLmax} = 0.45\text{ V}$ $V_{OHmin} = 1.35\text{ V}$	1.8 V power domain. If unused, keep these pins open.
DCD	38	DO	Data carrier detect		
CTS	36	DO	DTE clear to send signal from DCE	$V_{OLmax} = 0.45\text{ V}$ $V_{OHmin} = 1.35\text{ V}$	Connect to DTE's CTS. 1.8 V power domain. If unused, keep it open.
RTS	37	DI	DTE request to	$V_{ILmin} = -0.3\text{ V}$	Connect to DTE's

			send signal to DTE	$V_{ILmax} = 0.6\text{ V}$ $V_{IHmin} = 1.2\text{ V}$ $V_{IHmax} = 2.0\text{ V}$	RTS. 1.8 V power domain. If unused, keep it open.
DTR	30	DI	Data terminal ready Sleep mode control	$V_{ILmin} = -0.3\text{ V}$ $V_{ILmax} = 0.6\text{ V}$ $V_{IHmin} = 1.2\text{ V}$ $V_{IHmax} = 2.0\text{ V}$	1.8 V power domain. Pull-up by default. Low level wakes up the module. If unused, keep it open.
TXD	35	DO	Transmit	$V_{OLmax} = 0.45\text{ V}$ $V_{OHmin} = 1.35\text{ V}$	1.8 V power domain. If unused, keep these pins open.
RXD	34	DI	Receive	$V_{ILmin} = -0.3\text{ V}$ $V_{ILmax} = 0.6\text{ V}$ $V_{IHmin} = 1.2\text{ V}$ $V_{IHmax} = 2.0\text{ V}$	

**Debug UART Interface**

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
DBG_TXD	23	DO	Debug UART transmit	$V_{OLmax} = 0.45\text{ V}$ $V_{OHmin} = 1.35\text{ V}$	1.8 V power domain. If unused, keep these pins open.
DBG_RXD	22	DI	Debug UART receive	$V_{ILmin} = -0.3\text{ V}$ $V_{ILmax} = 0.6\text{ V}$ $V_{IHmin} = 1.2\text{ V}$ $V_{IHmax} = 2.0\text{ V}$	

**PCM Interface**

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
PCM_DIN	6	DI	PCM data input	$V_{ILmin} = -0.3\text{ V}$ $V_{ILmax} = 0.6\text{ V}$ $V_{IHmin} = 1.2\text{ V}$ $V_{IHmax} = 2.0\text{ V}$	1.8 V power domain. If unused, keep these pins open.
PCM_DOUT	7	DO	PCM data output	$V_{OLmax} = 0.45\text{ V}$ $V_{OHmin} = 1.35\text{ V}$	
PCM_SYNC	5	DIO	PCM data frame sync	$V_{OLmax} = 0.45\text{ V}$ $V_{OHmin} = 1.35\text{ V}$ $V_{ILmin} = -0.3\text{ V}$	1.8 V power domain. In master mode, it is an output signal. In slave mode, it is an input signal. If unused, keep these pins open.
PCM_CLK	4	DIO	PCM clock	$V_{ILmax} = 0.6\text{ V}$ $V_{IHmin} = 1.2\text{ V}$ $V_{IHmax} = 2.0\text{ V}$	

I2C Interface					
Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
I2C_SCL	40	OD	I2C serial clock (for external codec)		An external pull-up to 1.8 V is required.
I2C_SDA	41	OD	I2C serial data (for external codec)		If unused, keep these pins open.
ADC Interface					
Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
ADC0	24	AI	General-purpose ADC interface	Voltage range: 0.3 V to VBAT_BB	If unused, keep it open.
SPI Interface					
Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
SPI_CLK	26	DO	SPI clock	$V_{OLmax} = 0.45\text{ V}$	1.8 V power domain. If unused, keep these pins open.
SPI_MOSI	27	DO	SPI master-out slave-in	$V_{OHmin} = 1.35\text{ V}$	
SPI_MISO	28	DI	SPI master-in slave-out	$V_{ILmin} = -0.3\text{ V}$ $V_{ILmax} = 0.6\text{ V}$ $V_{IHmin} = 1.2\text{ V}$ $V_{IHmax} = 2.0\text{ V}$	
RF Antenna Interfaces					
Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
ANT_GNSS <sup>7</sup>	49	AI	GNSS antenna interface		50 $\Omega$ impedance. If unused, keep these pins open.
ANT_DIV <sup>8</sup>	56	AI	Diversity antenna interface		
ANT_MAIN	60	AIO	Main antenna interface		50 $\Omega$ impedance.
Other Pins					
Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
W_DISABLE#	18	DI	Airplane mode	$V_{ILmin} = -0.3\text{ V}$	1.8 V power domain.

<sup>7</sup> Pin 49 is defined as ANT\_GNSS on EG95-NA/-EX/-NAX/-NAXD/-AUX, while it is defined as ANT\_DIV on EG95-E.

<sup>8</sup> Pin 56 is RESERVED on EG95-E, while is defined as ANT\_DIV on EG95-NA/-EX/-NAX/-NAXD/-AUX.

			control	$V_{ILmax} = 0.6\text{ V}$ $V_{IHmin} = 1.2\text{ V}$ $V_{IHmax} = 2.0\text{ V}$	Pull-up by default. At low voltage level, module can enter airplane mode. If unused, keep it open.
AP_READY	19	DI	Application processor sleep state detection		1.8 V power domain. If unused, keep it open.
USB_BOOT	75	DI	Force the module to enter emergency download mode		1.8 V power domain. It is recommended to reserve the test points.

**RESERVED Pins**

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
NC	1, 2, 11–14, 16, 51, 57, 63–66, 76–78, 88, 92–99				Keep these pins unconnected.
RESERVED	25, 56				Keep these pins unconnected. Pin 56 is only reserved on EG95-E.

**NOTE**

1. Keep all RESERVED pins and unused pins unconnected.
2. BOOT\_CONFIG pins (SPI\_CLK, USB\_BOOT, PCM\_CLK, PCM\_SYNC) cannot be pulled up before startup.

### 3.4. Operating Modes

The following table briefly outlines the operating modes to be mentioned in the following chapters.

**Table 6: Overview of Operating Modes**

Mode	Details	
Normal Operation	Idle	Software is active. The module has registered on the network, and it is ready to send and receive data.

	Talk/Data	Network is connected. In this mode, the power consumption is decided by network setting and data transfer rate.
Airplane Mode		<b>AT+CFUN=4</b> or W_DISABLE# pin can set the module to enter airplane mode. In this case, RF function will be invalid.
Minimum Functionality Mode		<b>AT+CFUN=0</b> can set the module to a minimum functionality mode without removing the power supply. In this case, both RF function and (U)SIM card will be invalid.
Sleep Mode		In this mode, the current consumption of the module will be reduced to the minimal level. During this mode, the module can still receive paging message, SMS, voice call and TCP/UDP data from the network normally.
Power Down Mode		In this mode, the power management unit shuts down the power supply. Software goes inactive. The serial interface is not accessible. Operating voltage (connected to VBAT_RF and VBAT_BB) remains applied.

### 3.5. Power Saving

#### 3.5.1. Sleep Mode

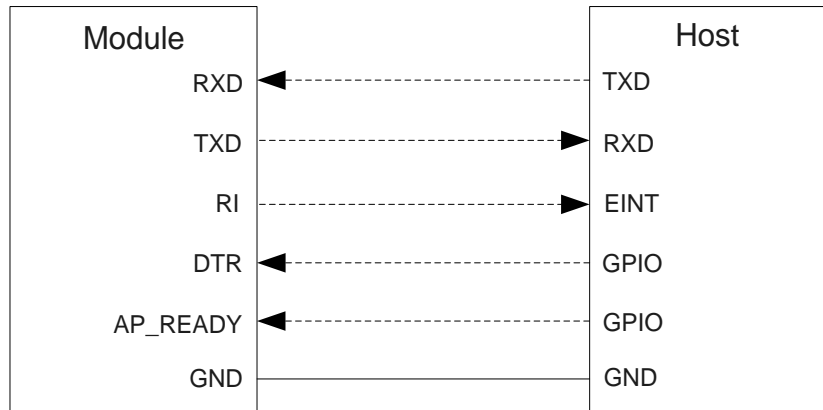
EG95 series module is able to reduce its current consumption to a minimum value during the sleep mode. The following sub-chapters describe the power saving procedures of EG95 series module.

##### 3.5.1.1. UART Application

If the host communicates with module via UART interface, the following preconditions can let the module enter sleep mode.

- Execute **AT+QSCLK=1** to enable sleep mode.
- Drive DTR to high level.

The following figure shows the connection between the module and the host.



**Figure 3: Sleep Mode Application via UART**

Driving the host DTR to low level will wake up the module.

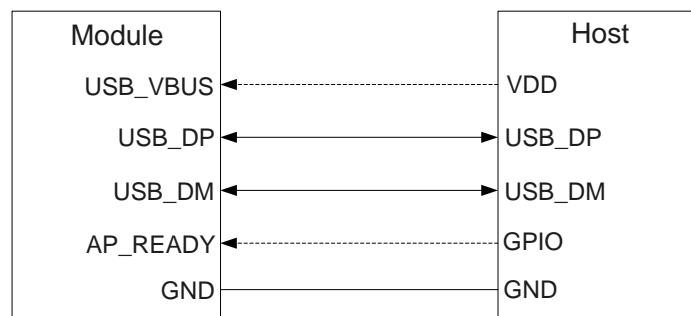
- When EG95 series module has a URC to report, RI signal will wake up the host. See **Chapter 3.15.3** for details about RI behaviors.
- AP\_READY will detect the sleep state of host (can be configured to high level or low level detection). See **AT+QCFG="apready"** for details.

**3.5.1.2. USB Application with USB Remote Wakeup Function**

If the host supports USB suspend/resume and remote wakeup functions, the following three preconditions must be met to let the module enter sleep mode.

- Execute **AT+QSCLK=1** to enable sleep mode.
- Ensure the DTR is held at high level or keep it open.
- The host’s USB bus, which is connected with the module’s USB interface, enters suspend state.

The following figure shows the connection between the module and the host.



**Figure 4: Sleep Mode Application with USB Remote Wakeup**

- Sending data to EG95 series module through USB will wake up the module.
- When EG95 series module has a URC to report, the module will send remote wakeup signals via USB bus to wake up the host.

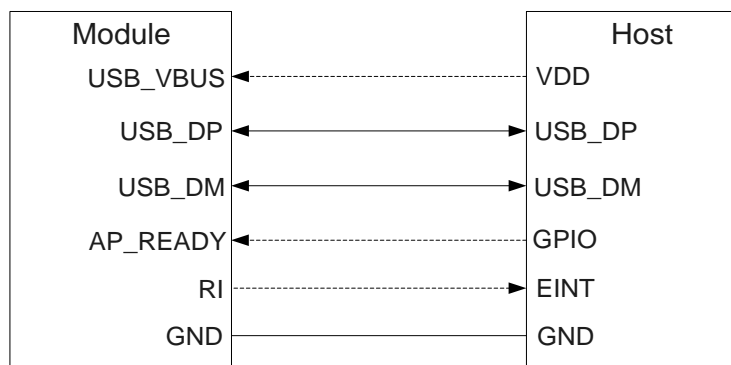
**3.5.1.3. USB Application with USB Suspend/Resume and RI Function**

If the host supports USB suspend/resume, but does not support remote wake-up function, the RI signal is needed to wake up the host.

There are three preconditions to let the module enter sleep mode.

- Execute **AT+QSCLK=1** to enable sleep mode.
- Ensure the DTR is held at high level or keep it open.
- The host’s USB bus, which is connected with the module’s USB interface, enters suspended state.

The following figure shows the connection between the module and the host.



**Figure 5: Sleep Mode Application with RI**

- Sending data to EG95 series module via USB will wake up the module.
- When module has a URC to report, RI signal will wake up the host.

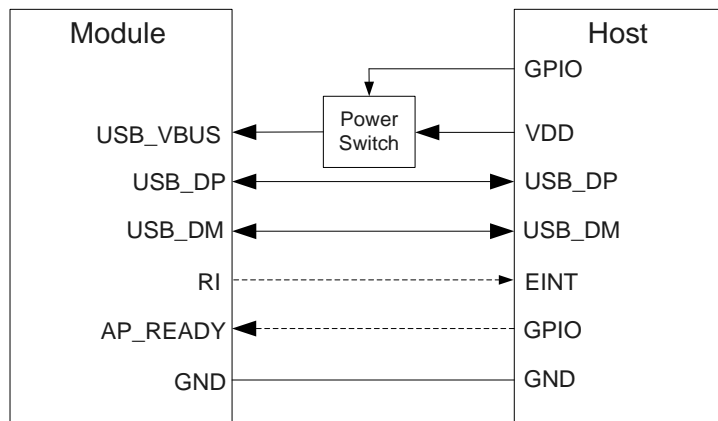
**3.5.1.4. USB Application without USB Suspend Function**

If the host does not support USB suspend function, USB\_VBUS should be disconnected with an external control circuit to let the module enter sleep mode.

- Execute **AT+QSCLK=1** to enable the sleep mode.
- Ensure the DTR is held at high level or keep it open.
- Disconnect USB\_VBUS.



The following figure shows the connection between the module and the host.



**Figure 6: Sleep Mode Application without Suspend Function**

Switching on the power switch to supply power to USB\_VBUS will wake up the module.

**NOTE**

1. Pay attention to the level match shown in dotted line between the module and the host. See **document [2]** for more details about EG95 series module power management application.
2. For details of **AT+QSCCLK**, see **document [3]**.
3. For details of **AT+QCFG**, see **document [5]**.

### 3.5.2. Airplane Mode

When the module enters airplane mode, the RF function will be disabled, and all AT commands related to it will be inaccessible. This mode can be set via the following ways.

**Hardware:**

The W\_DISABLE# pin is pulled up by default. Driving it to low level will let the module enter airplane mode.

**Software:**

**AT+CFUN=<fun>** provides the choice of the functionality level through setting <fun> as 0, 1 or 4.

- **AT+CFUN=0**: Minimum functionality mode. Both (U)SIM and RF functions are disabled.
- **AT+CFUN=1**: Full functionality mode (by default).
- **AT+CFUN=4**: Airplane mode. RF function is disabled.

**NOTE**

1. Airplane mode control via W\_DISABLE# is disabled in firmware by default. It can be enabled by **AT+QCFG="airplanecontrol"**.
2. The execution of **AT+CFUN** will not affect GNSS function.

### 3.6. Power Supply

#### 3.6.1. Power Supply Pins

EG95 series module provides four VBAT pins for connection with the external power supply. There are two separate voltage domains for VBAT.

- Two VBAT\_RF pins for module’s RF part.
- Two VBAT\_BB pins for module’s baseband part.

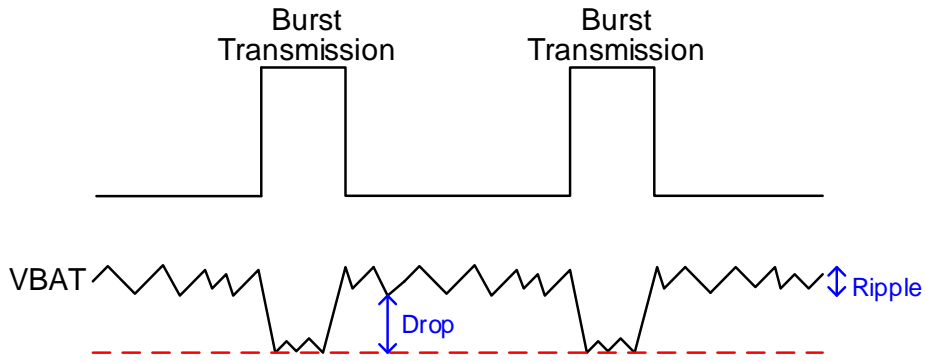
The following table shows the details of VBAT pins and ground pins.

**Table 7: Pin Definition of VBAT and GND Pins**

Pin Name	Pin No.	Description	Min.	Typ.	Max.	Unit
VBAT_RF	52, 53	Power supply for module’s RF part.	3.3	3.8	4.3	V
VBAT_BB	32, 33	Power supply for module’s baseband part.	3.3	3.8	4.3	V
GND	3, 31, 48, 50, 54, 55, 58, 59, 61, 62, 67–74, 79–82, 89–91, 100–106		-	0	-	V

#### 3.6.2. Voltage Stability Requirements

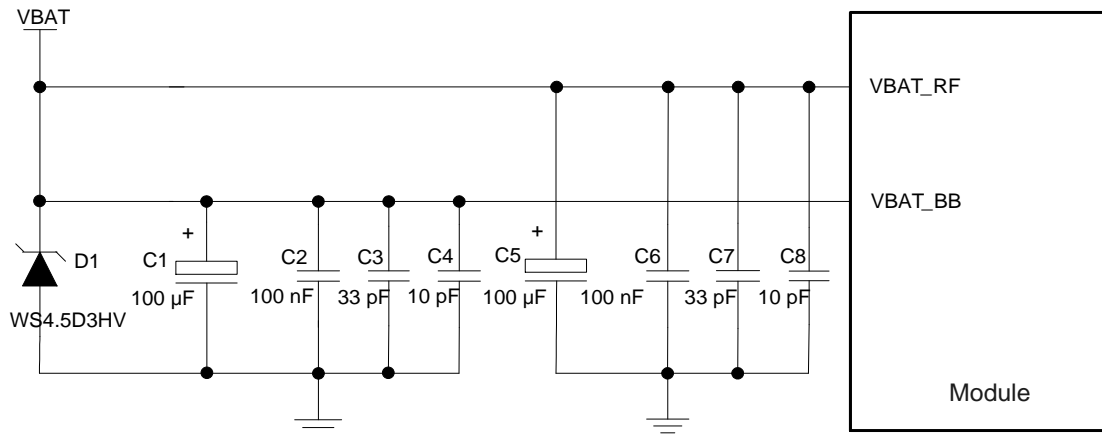
The power supply range of the module is from 3.3 V to 4.3 V. Please make sure that the input voltage will never drop below 3.3 V. The following figure shows the voltage drop during burst transmission in 2G network. The voltage drop will be less in 3G and 4G networks.



**Figure 7: Power Supply Limits during Burst Transmission**

To decrease voltage drop, a bypass capacitor of about 100  $\mu\text{F}$  with low ESR ( $\text{ESR} = 0.7 \Omega$ ) should be used, and a multi-layer ceramic chip (MLCC) capacitor array should also be reserved due to its ultra-low ESR. It is recommended to use three ceramic capacitors (100 nF, 33 pF, 10 pF) for composing the MLCC array, and place these capacitors close to VBAT\_BB/VBAT\_RF pins. The main power supply from an external application has to be a single voltage source and can be expanded to two sub paths with star structure. The width of VBAT\_BB trace should be no less than 1 mm, and the width of VBAT\_RF trace should be no less than 2 mm. In principle, the longer the VBAT trace is, the wider it will be.

In addition, to avoid the damage caused by electric surge and ESD, it is suggested that a TVS diode with suggested low reverse stand-off voltage  $V_{\text{RWM}}$  (4.5 V), low clamping voltage  $V_{\text{C}}$  and high reverse peak pulse current  $I_{\text{PP}}$  should be used. The following figure shows the star structure of the power supply.

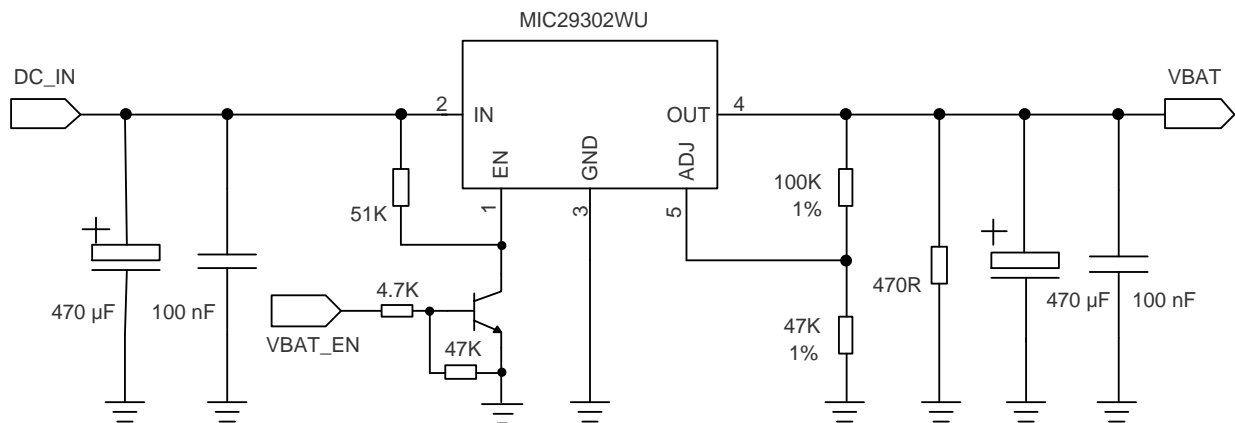


**Figure 8: Star Structure of Power Supply**

### 3.6.3. Reference Design for Power Supply

Power design for the module is very important, as the performance of the module largely depends on the power source. The power supply should be able to provide sufficient current up to 2 A at least. If the voltage drop between the input and output is not too high, it is suggested that an LDO should be used to supply power for the module. If there is a big voltage difference between the input source and the desired output (VBAT), a buck converter is preferred to be used as the power supply.

The following figure shows a reference design for +5 V input power source. The typical output of the power supply is about 3.8 V and the maximum load current is 3.0 A.



**Figure 9: Reference Circuit of Power Supply**

**NOTE**

To avoid corrupting the data of internal flash, do not switch off the power supply when the module works normally. Only after the module is shut down by PWRKEY or AT command, then the power supply can be cut off.

### 3.6.4. Power Supply Voltage Monitoring

AT+CBC can be used to monitor the VBAT\_BB voltage value. For more details, see *document [3]*.

## 3.7. Turn on

### 3.7.1. Turn on with PWRKEY

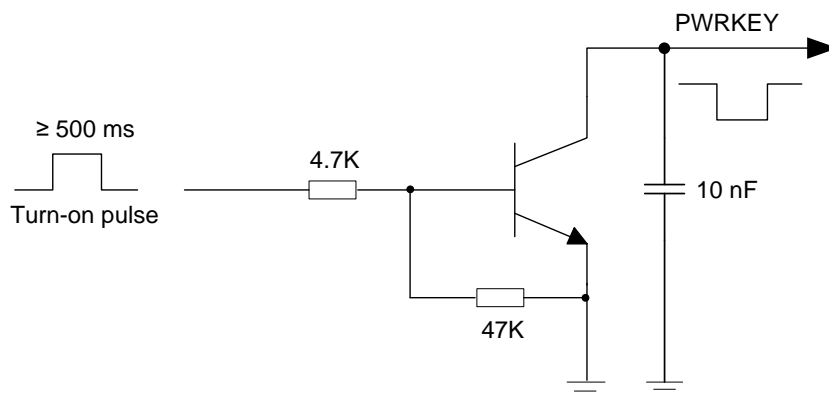
The following table shows the pin definition of PWRKEY.

**Table 8: Pin Definition of PWRKEY**

Pin Name	Pin No.	Description	Comment
PWRKEY	15	Turn on/off the module	The output voltage is 0.8 V because of the diode drop in the baseband chipset.

When EG95 series module is in power down mode, it can be turned on to normal mode by driving the PWRKEY low for at least 500 ms. It is recommended to use an open drain/collector driver to control the PWRKEY. After STATUS pin outputting a high level, PWRKEY pin can be released.

A simple reference circuit is illustrated in the following figure.



**Figure 10: Turn on the Module by Using Driving Circuit**

The other way to control the PWRKEY is using a button directly. When pressing the button, electrostatic strike may generate from the finger. Therefore, a TVS component is indispensable to be placed nearby the button for ESD protection. A reference circuit is shown in the following figure.

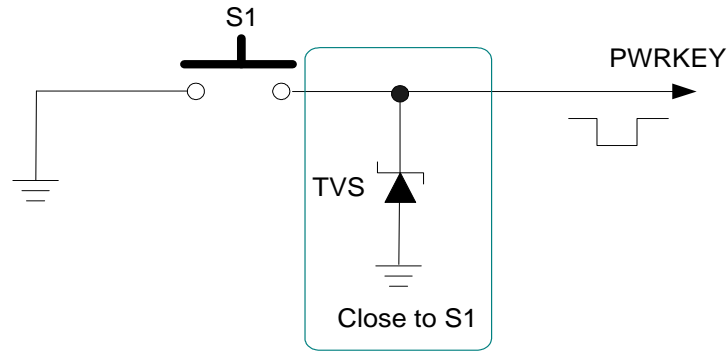


Figure 11: Turn on the Module by Using a Button

The power-up scenario is illustrated in the following figure.

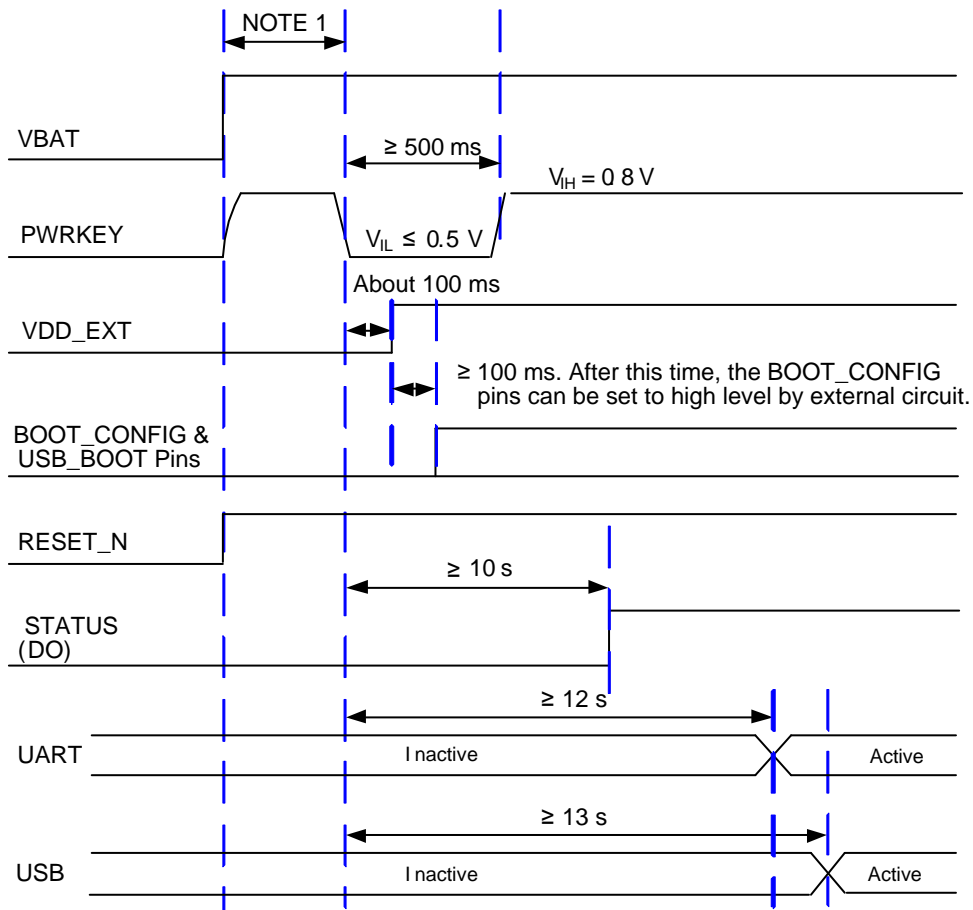


Figure 12: Power-up Timing

**NOTE**

1. Make sure that VBAT is stable before pulling down PWRKEY pin. It is recommended that the time between powering up VBAT and pulling down PWRKEY pin is no less than 30 ms.

2. PWRKEY can be pulled down directly to GND with a recommended 10 kΩ resistor if module needs to be powered on automatically and shutdown is not needed.
3. BOOT\_CONFIG pins (SPI\_CLK, USB\_BOOT, PCM\_CLK, PCM\_SYNC) cannot be pulled up before startup.

### 3.8. Turn off

The following procedures can be used to turn off the module normally:

- Use the PWRKEY pin.
- Use **AT+QPOWD**.

#### 3.8.1. Turn off with PWRKEY

Driving PWRKEY low for at least 650 ms, the module will execute power-off procedure after the PWRKEY is released. The power-down scenario is illustrated in the following figure.

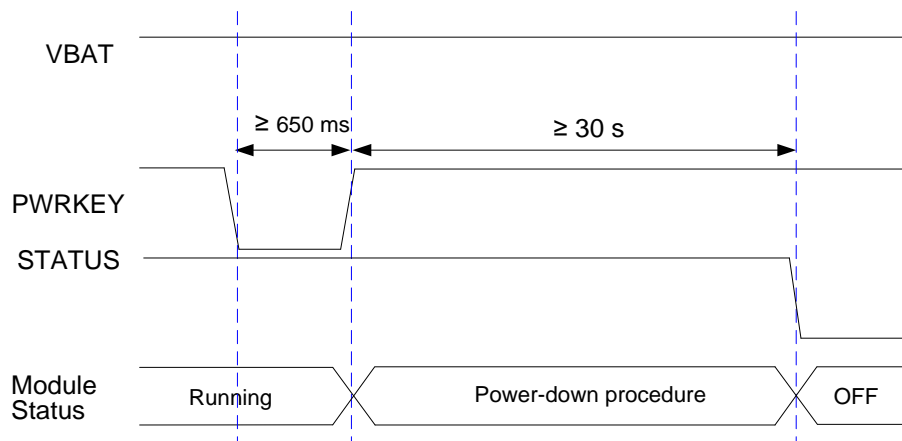


Figure 13: Power-down Timing

#### 3.8.2. Turn off with AT Command

It is also a safe way to use **AT+QPOWD** to turn off the module, which is similar to turning off the module via PWRKEY pin.

See *document [3]* for details about the **AT+QPOWD**.

**NOTE**

1. To avoid corrupting the data of internal flash, do not switch off the power supply when the module works normally. Only after the module is shut down by PWRKEY or AT command, then the power supply can be cut off.
2. When turning off module with the AT command, keep PWRKEY at high level after the execution of the command. Otherwise the module will be turned on again after successfully turn-off.

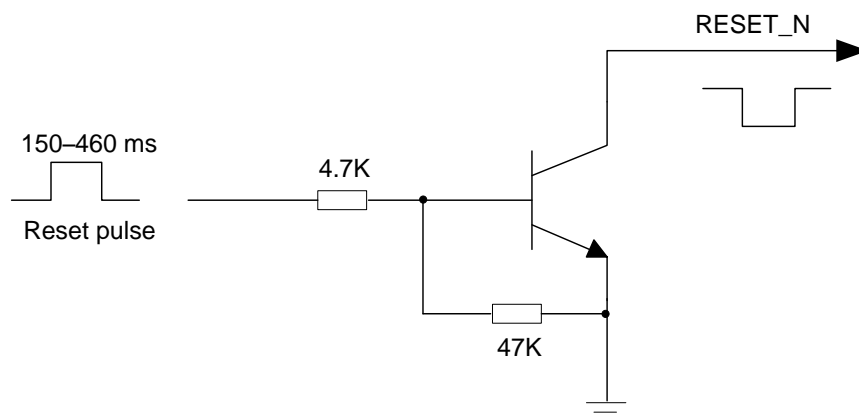
### 3.9. Reset

The RESET\_N pin can be used to reset the module. The module can be reset by driving RESET\_N to a low level voltage for 150–460 ms.

**Table 9: Pin Definition of RESET\_N**

Pin Name	Pin No.	Description	Comment
RESET_N	17	Reset the module	Pull-up to 1.8 V internally. Active LOW. If unused, keep it open.

The recommended circuit is similar to the PWRKEY control circuit. An open drain/collector driver or button can be used to control the RESET\_N.



**Figure 14: Reference Circuit of RESET\_N by Using Driving Circuit**



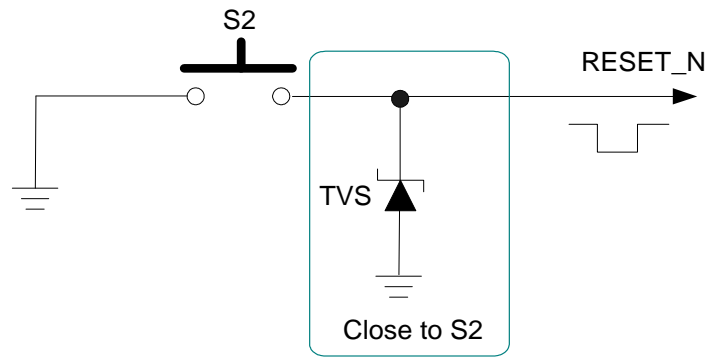


Figure 15: Reference Circuit of RESET\_N by Using Button

The reset scenario is illustrated in the following figure.

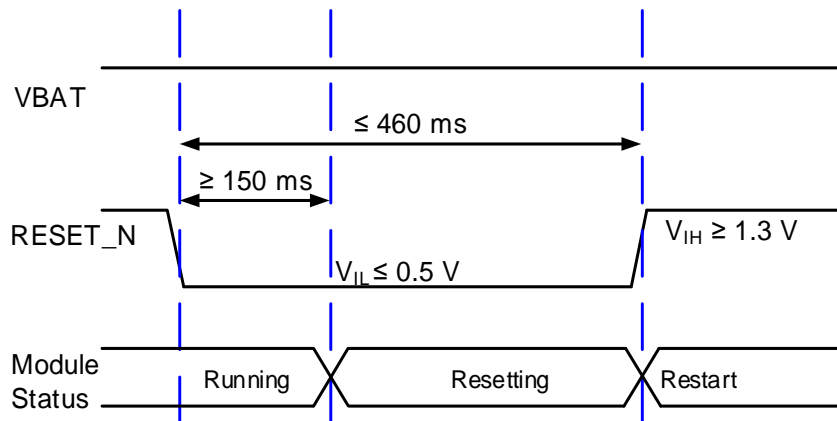


Figure 16: Reset Timing

**NOTE**

1. Use RESET\_N only when failed to turn off the module by **AT+QPOWD** and PWRKEY pin.
2. Ensure that there is no large capacitance on PWRKEY and RESET\_N pins.

### 3.10. (U)SIM Interfaces

EG95 series module provides two (U)SIM interfaces, and only one (U)SIM card can work at a time. The (U)SIM1 and (U)SIM2 cards can be switched by **AT+QDSIM**. For more details, see **document [3]**.

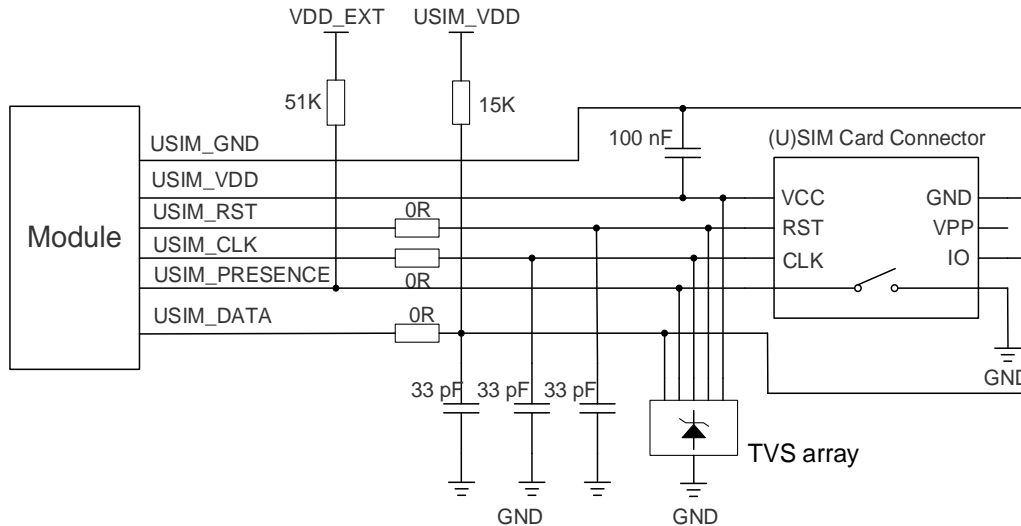
The (U)SIM interfaces circuitry meet ETSI and IMT-2000 requirements. Both 1.8 V and 3.0 V (U)SIM cards are supported.

**Table 10: Pin Definition of (U)SIM Interfaces**

Pin Name	Pin No.	I/O	Description	Comment
USIM1_VDD	43	PO	(U)SIM1 card power supply	Either 1.8 V or 3.0 V is supported by the module automatically.
USIM1_DATA	45	DIO	(U)SIM1 card data	
USIM1_CLK	46	DO	(U)SIM1 card clock	
USIM1_RST	44	DO	(U)SIM1 card reset	
USIM1_PRESENCE	42	DI	(U)SIM1 card hot plug detection	
USIM_GND	47		Specified ground for (U)SIM card	
USIM2_VDD	87	PO	(U)SIM2 card power supply	Either 1.8 V or 3.0 V is supported by the module automatically. If unused, keep it open.
USIM2_DATA	86	DIO	(U)SIM2 card data	
USIM2_CLK	84	DO	(U)SIM2 card clock	
USIM2_RST	85	DO	(U)SIM2 card reset	
USIM2_PRESENCE	83	DI	(U)SIM2 card hot plug detection	

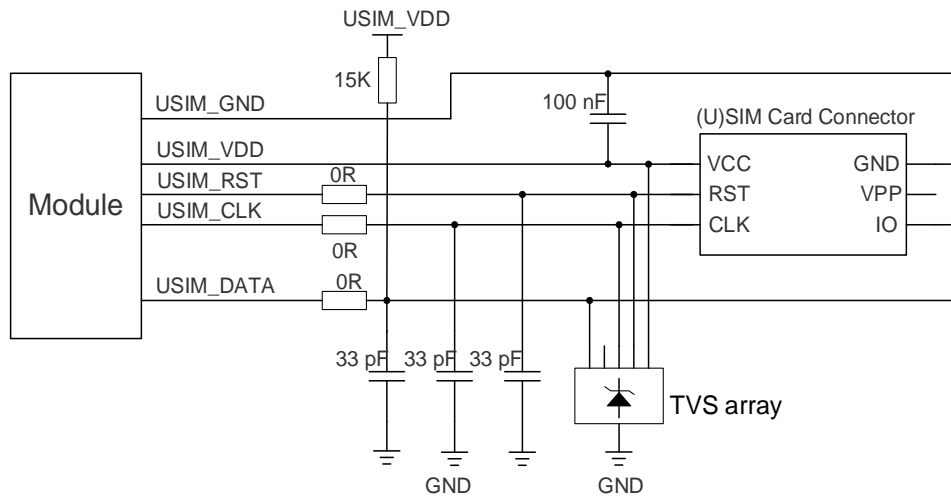
EG95 series module supports (U)SIM card hot-plug via USIM\_PRESENCE pin, and both high and low level detection are supported. The function is disabled by default, and see **document [3]** for more details about **AT+QSIMDET**.

The following figure shows a reference design for (U)SIM interface with an 8-pin (U)SIM card connector.



**Figure 17: Reference Circuit of (U)SIM Interface with an 8-pin (U)SIM Card Connector**

If (U)SIM card detection function is not needed, keep USIM\_PRESENCE unconnected. A reference circuit of (U)SIM interface with a 6-pin (U)SIM card connector is illustrated in the following figure.



**Figure 18: Reference Circuit of (U)SIM Interface with a 6-pin (U)SIM Card Connector**

To enhance the reliability and availability of the (U)SIM cards in your applications, follow the criteria below in the (U)SIM circuit design:

- Keep placement of (U)SIM card connector to the module as close as possible. Keep the trace length as less than 200 mm as possible.
- Keep (U)SIM card signals away from RF and power supply traces.
- Make sure the bypass capacitor between USIM\_VDD and USIM\_GND less than 1  $\mu$ F, and place it as close to (U)SIM card connector as possible. If the ground is complete on your PCB, USIM\_GND can be connected to PCB ground directly.

- To avoid cross-talk between USIM\_DATA and USIM\_CLK, keep them away from each other and shield them with surrounded ground.
- For better ESD protection, it is recommended to add a TVS array whose parasitic capacitance should not be more than 15 pF. The 0 Ω resistors should be added in series between the module and the (U)SIM card to facilitate debugging. The 33 pF capacitors are used for filtering interference of EGSM900. Please note that the (U)SIM peripheral circuit should be close to the (U)SIM card connector.
- The pull-up resistor on USIM\_DATA trace can improve anti-jamming capability when long layout trace and sensitive occasion are applied, and should be placed close to the (U)SIM card connector.

### 3.11. USB Interface

EG95 series module contains one integrated Universal Serial Bus (USB) interface which complies with the USB 2.0 specification and supports high-speed (480 Mbps) and full-speed (12 Mbps) modes.

The USB interface can only serves as a slave device and is used for AT command communication, data transmission, GNSS NMEA sentences output, software debugging, firmware upgrade and voice over USB.

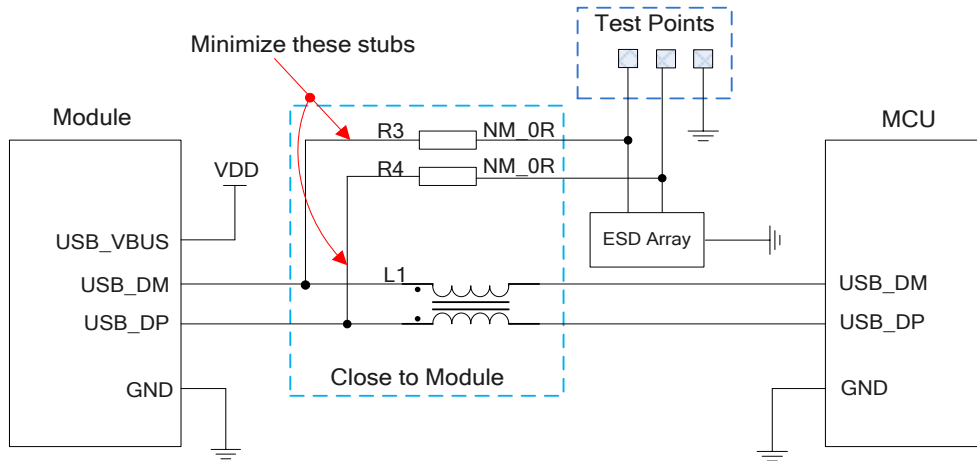
The following table shows the pin definition of USB interface.

**Table 11: Pin Definition of USB Interface**

Pin Name	Pin No.	I/O	Description	Comment
USB_DP	9	AIO	USB differential data (+)	USB 2.0 compliant.
USB_DM	10	AIO	USB differential data (-)	Require differential impedance of 90 Ω.
USB_VBUS	8	PI	USB connection detect	Typical: 5.0 V
GND	3		Ground	

For more details about USB 2.0 specifications, visit <http://www.usb.org/home>.

The USB interface is recommended to be reserved for firmware upgrade in your design. The following figure shows a reference circuit of USB interface.



**Figure 19: Reference Circuit of USB Interface**

A common mode choke L1 is recommended to be added in series between the module and your MCU to suppress EMI spurious transmission. Meanwhile, the 0 Ω resistors (R3 and R4) should be added in series between the module and the test points to facilitate debugging, and the resistors are not mounted by default. To ensure the integrity of USB data line signal, L1/R3/R4 components must be placed close to the module, and also these resistors should be placed close to each other. The extra stubs of trace must be as short as possible.

To meet USB 2.0 specification, the following principles should be complied with when design the USB interface.

- It is important to route the USB signal traces as differential pairs with ground surrounded. The impedance of USB differential trace is 90 Ω.
- Do not route signal traces under crystals, oscillators, magnetic devices and RF signal traces. It is important to route the USB differential traces in inner-layer of the PCB, and surround the traces with ground on that layer and with ground planes above and below.
- Junction capacitance of the ESD protection component might cause influences on USB data traces, so pay attention to the selection of the device. Typically, the stray capacitance should be less than 2 pF.
- Keep the ESD protection components as close to the USB connector as possible.

### 3.12. UART Interfaces

The module provides two UART interfaces: the main UART interface and the debug UART interface. The following shows their features.

- The main UART interface supports 9600 bps, 19200 bps, 38400 bps, 57600 bps, 115200 bps, 230400 bps, 460800 bps and 921600 bps baud rates, and the default is 115200 bps. It supports RTS and CTS hardware flow control, and is used for AT command communication and data transmission.
- The debug UART interface supports 115200 bps baud rate. It is used for Linux console and log output.

The following tables show the pin definition of the UART interfaces.

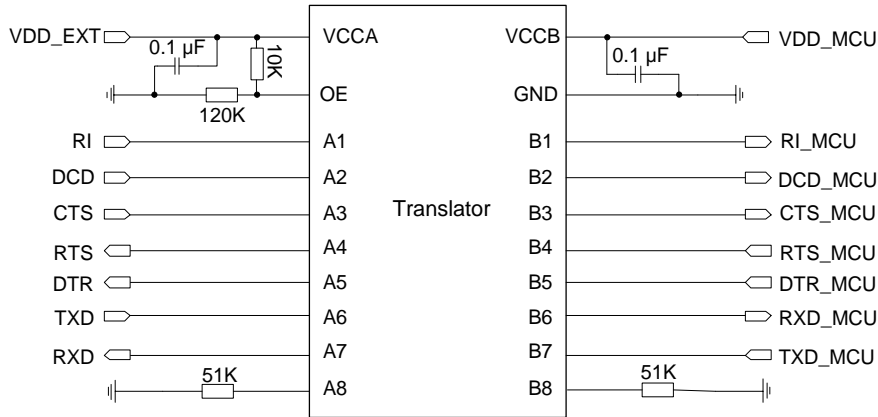
**Table 12: Pin Definition of Main UART Interface**

Pin Name	Pin No.	I/O	Description	Comment
RI	39	DO	Ring indication	1.8 V power domain If unused, keep these pins open.
DCD	38	DO	Data carrier detect	
CTS	36	DO	DTE clear to send signal from DCE	Connect to DTE's CTS. 1.8 V power domain If unused, keep it open.
RTS	37	DI	DTE request to send signal to DTE	Connect to DTE's RTS. 1.8 V power domain If unused, keep it open.
DTR	30	DI	Data terminal ready Sleep mode control	1.8 V power domain If unused, keep it open.
TXD	35	DO	Transmit	
RXD	34	DI	Receive	

**Table 13: Pin Definition of Debug UART Interface**

Pin Name	Pin No.	I/O	Description	Comment
DBG_TXD	23	DO	Debug UART transmit	1.8 V power domain
DBG_RXD	22	DI	Debug UART receive	

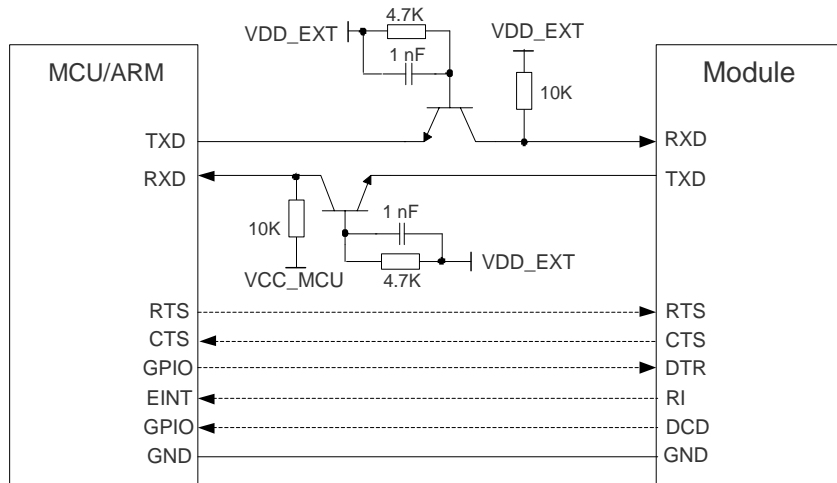
The module provides 1.8 V UART interfaces. A voltage-level translator should be used if your application is equipped with a 3.3 V UART interface. A voltage-level translator TXS0108EPWR provided by Texas Instruments is recommended. The following figure shows a reference design.



**Figure 20: Reference Circuit with Translator Chip**

Visit <http://www.ti.com> for more information.

Another example with transistor translation circuit is shown as below. For the design of circuits in dotted lines, see that of circuits in solid lines, but pay attention to the direction of connection.



**Figure 21: Reference Circuit with Transistor Circuit**

**NOTE**

1. Transistor circuit solution is not suitable for applications with high baud rates exceeding 460 kbps.
2. Please note that the module's CTS is connected to the host's CTS, and the module's RTS is connected to the hosts's RTS.

### 3.13. PCM and I2C Interfaces

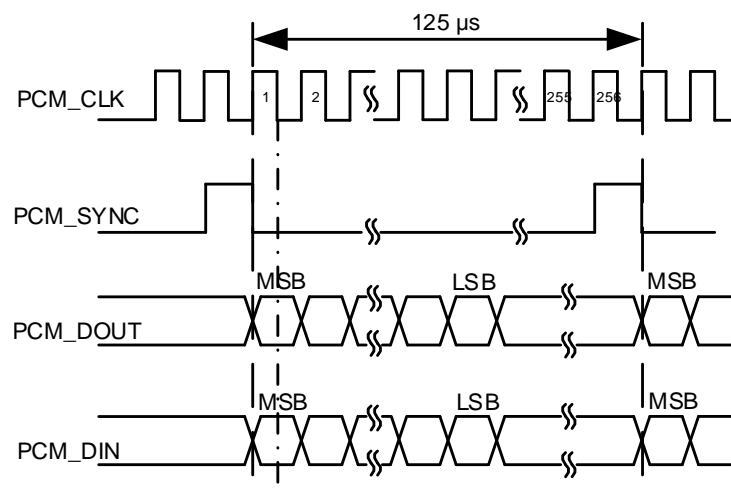
EG95 series module provides one Pulse Code Modulation (PCM) digital interface for audio design, which supports the following modes and one I2C interface:

- Primary mode (short frame synchronization, works as both master and slave)
- Auxiliary mode (long frame synchronization, works as master only)

In primary mode, the data is sampled on the falling edge of the PCM\_CLK and transmitted on the rising edge. The PCM\_SYNC falling edge represents the MSB. In this mode, the PCM interface supports 256 kHz, 512 kHz, 1024 kHz or 2048 kHz PCM\_CLK at 8 kHz PCM\_SYNC, and also supports 4096 kHz PCM\_CLK at 16 kHz PCM\_SYNC.

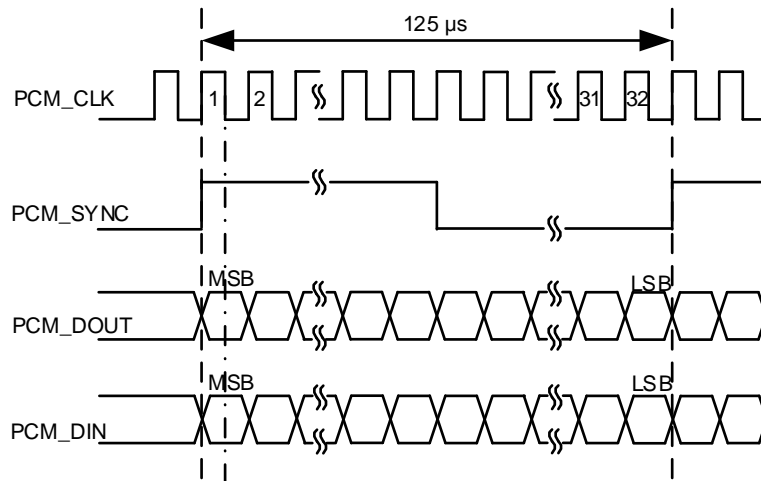
In auxiliary mode, the data is also sampled on the falling edge of the PCM\_CLK and transmitted on the rising edge. The PCM\_SYNC rising edge represents the MSB. In this mode, the PCM interface operates with a 256 kHz, 512 kHz, 1024 kHz or 2048 kHz PCM\_CLK and an 8 kHz, 50 % duty cycle PCM\_SYNC.

EG95 series module supports 16-bit linear data format. The following figures show the primary mode's timing relationship with 8 kHz PCM\_SYNC and 2048 kHz PCM\_CLK, as well as the auxiliary mode's timing relationship with 8 kHz PCM\_SYNC and 256 kHz PCM\_CLK.



**Figure 22: Primary Mode Timing**





**Figure 23: Auxiliary Mode Timing**

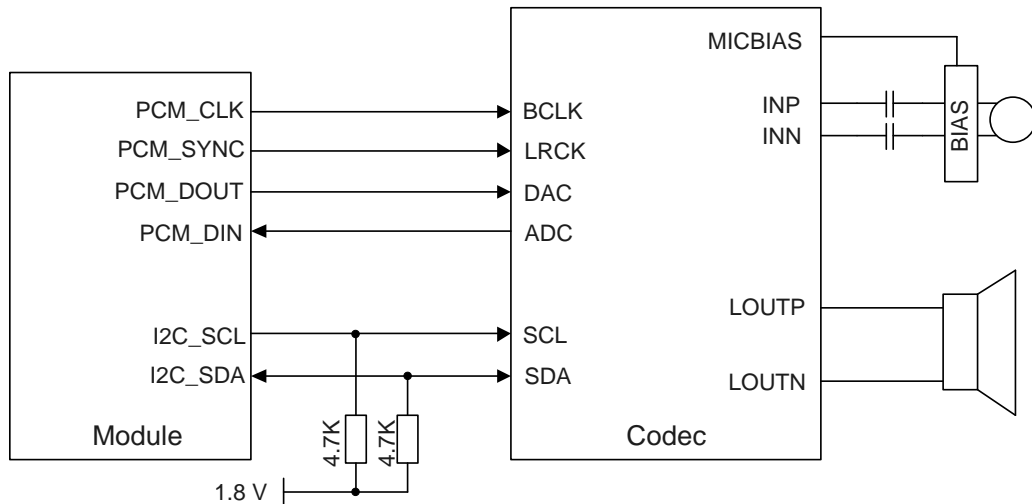
The following table shows the pin definition of PCM and I2C interfaces which can be applied on audio codec design.

**Table 14: Pin Definition of PCM and I2C Interfaces**

Pin Name	Pin No.	I/O	Description	Comment
PCM_DIN	6	DI	PCM data input	1.8 V power domain
PCM_DOUT	7	DO	PCM data output	If unused, keep these pins open.
PCM_SYNC	5	DIO	PCM data frame sync	1.8 V power domain In master mode, it is an output signal.
PCM_CLK	4	DIO	PCM data clock	In slave mode, it is an input signal. If unused, keep these pins open.
I2C_SCL	40	OD	I2C serial clock (for external codec)	An external pull-up to 1.8 V is required.
I2C_SDA	41	OD	I2C serial data (for external codec)	

Clock and mode can be configured by AT command, and the default configuration is master mode using short frame synchronization format with 2048 kHz PCM\_CLK and 8 kHz PCM\_SYNC. See **document [3]** about **AT+QDAI** for details.

The following figure shows a reference design of PCM and I2C interfaces with external codec IC.



**Figure 24: Reference Circuit of PCM and I2C Application with Audio Codec**

**NOTE**

1. It is recommended to reserve an RC (R = 22 Ω, C = 22 pF) circuit on the PCM traces, especially for PCM\_CLK.
2. EG95 series module works as a master device pertaining to I2C interface.

### 3.14. SPI Interface

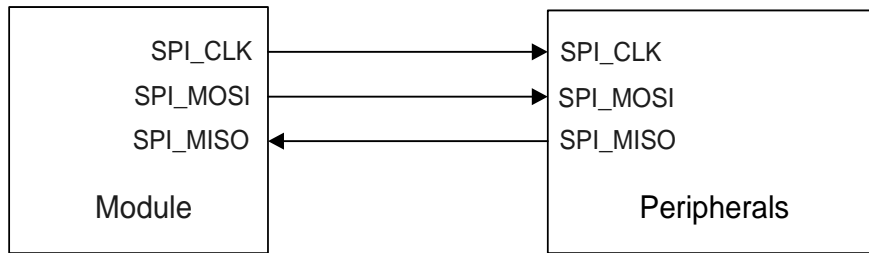
SPI interface only acts as master device. It provides a duplex, synchronous and serial communication link with the peripheral devices. It is dedicated to one-to-one connection, without chip selection. Its operation voltage is 1.8 V with clock rates up to 50 MHz.

The following table shows the pin definition of SPI interface.

**Table 15: Pin Definition of SPI Interface**

Pin Name	Pin No.	I/O	Description	Comment
SPI_CLK	26	DO	SPI clock	1.8 V power domain If unused, keep these pins open.
SPI_MOSI	27	DO	SPI master-out slave-in	
SPI_MISO	28	DI	SPI master-in slave-out	

The following figure shows a reference design of SPI interface with peripherals.



**Figure 25: Reference Circuit of SPI Interface with Peripherals**

**NOTE**

The module provides 1.8 V SPI interface. A voltage-level translator should be used between the module and the host if your application is equipped with a 3.3 V processor or device interface.

### 3.15. Indication Signals

#### 3.15.1. Network Status Indication

The module provides one network indication pin: NETLIGHT. The pin is used to indicate LED status.

The following tables describe the pin definition and logic level changes of NETLIGHT in different network status.

**Table 16: Pin Definition of Network Status Indicator**

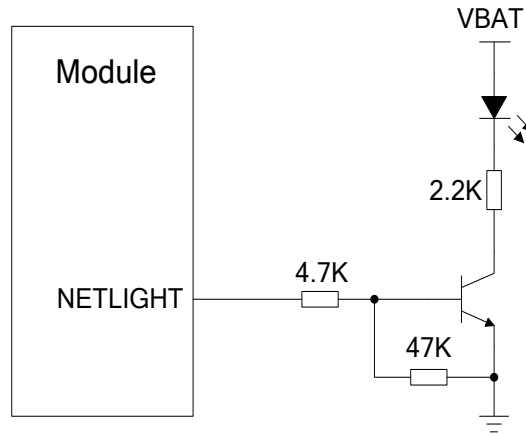
Pin Name	Pin No.	I/O	Description	Comment
NETLIGHT	21	DO	Indicate the module's network activity status	1.8 V power domain

**Table 17: Working State of Network Status Indicator**

Pin Name	Logic Level Changes	Network Status
NETLIGHT	Flicker slowly (200 ms High/1800 ms Low)	Network searching
	Flicker slowly (1800 ms High/200 ms Low)	Idle

Flicker quickly (125 ms High/125 ms Low)	Data transfer is ongoing
Always High	Voice calling

A reference circuit is shown in the following figure.



**Figure 26: Reference Circuit of Network Status Indicator**

### 3.15.2. STATUS

The STATUS pin is set as the module’s operation status indicator. It will output high level when the module is powered on. The following table describes the pin definition of STATUS.

**Table 18: Pin Definition of STATUS**

Pin Name	Pin No.	I/O	Description	Comment
STATUS	20	DO	Indicate the module’s operating status	1.8 V power domain. If unused, keep it open.

The following figure shows the reference circuit of STATUS.

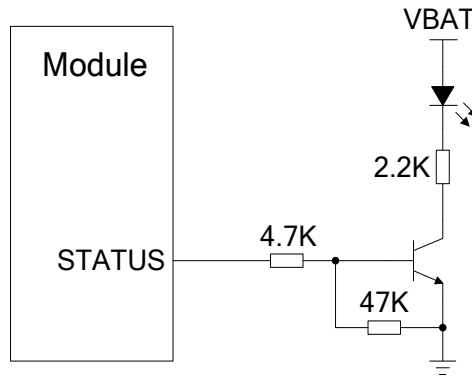


Figure 27: Reference Circuit of STATUS

### 3.15.3. RI

**AT+QCFG="risignaltpe","physical"** can be used to configure RI behaviors. See *document [5]* for details.

No matter on which port URC is presented, URC will trigger the behavior of RI pin.

**NOTE**

URC can be outputted from UART port, USB AT port and USB modem port through configuration via **AT+QURCCFG**. The default port is USB AT port.

The default behaviors of the RI are shown as below, and can be changed by **AT+QCFG="urc/ri/ring"**. See *document [5]* for details.

Table 19: Default Behaviors of RI

State	Response
Idle	RI keeps at high level
URC	RI outputs 120 ms low pulse when a new URC returns

### 3.16. ADC Interface

The module provides one analog-to-digital converter (ADC) interface. **AT+QADC=0** can be used to read the voltage value on ADC0 pin. For more details about the command, see **document [3]**.

To improve the accuracy of ADC voltage values, the traces of ADC should be surrounded by ground.

**Table 20: Pin Definition of ADC Interface**

Pin Name	Pin No.	I/O	Description	Comment
ADC0	24	AI	General purpose ADC interface	If unused, keep this pin open.

The following table describes the characteristics of ADC interface.

**Table 21: Characteristics of ADC Interface**

Parameter	Min.	Typ.	Max.	Unit
ADC0 Voltage Range	0.3	-	VBAT_BB	V
ADC Resolution	-	-	15	bits

**NOTE**

1. It is prohibited to supply any voltage to ADC pins when ADC pins are not powered by VBAT.
2. It is recommended to use resistor divider circuit for ADC application.

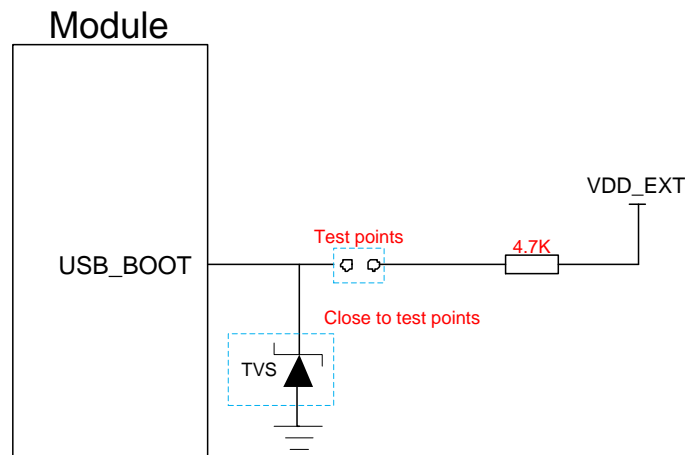
### 3.17. USB\_BOOT Interface

EG95 series module provides a USB\_BOOT pin. You can pull up USB\_BOOT to VDD\_EXT before VDD\_EXT is powered up, and the module will enter emergency download mode when it is powered on. In this mode, the module supports firmware upgrade over USB interface.

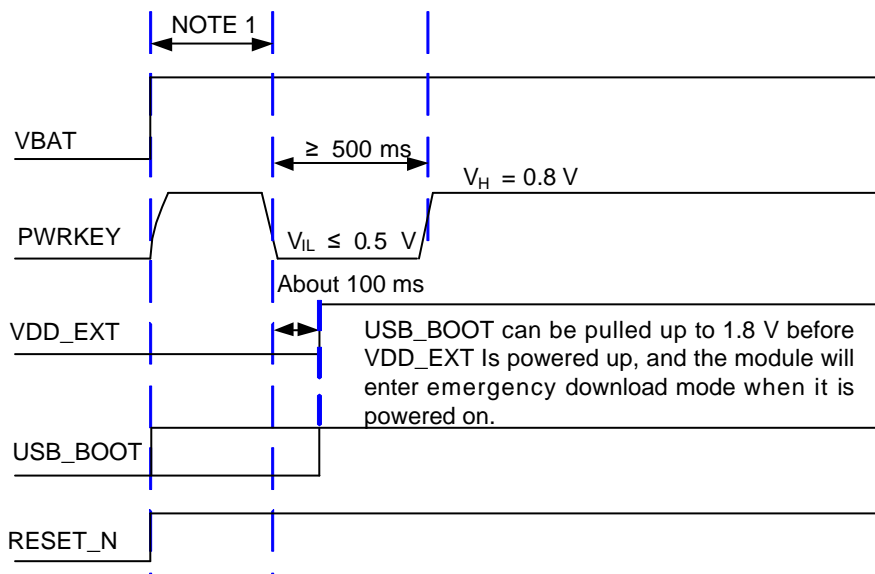
**Table 22: Pin Definition of USB\_BOOT Interface**

Pin Name	Pin No.	I/O	Description	Comment
USB_BOOT	75	DI	Force the module to enter emergency download mode	1.8 V power domain. Active HIGH. It is recommended to reserve test points.

The following figures show the reference circuit of USB\_BOOT interface and timing sequence of entering emergency download mode.



**Figure 28: Reference Circuit of USB\_BOOT Interface**



**Figure 29: Entering Emergency Download Mode Timing**

**NOTE**

1. Make sure that VBAT is stable before pulling down PWRKEY pin. It is recommended that the time between powering up VBAT and pulling down PWRKEY pin is no less than 30 ms.
2. When using MCU to control the module to enter the emergency download mode, follow the above timing sequence. It is not recommended to pull up USB\_BOOT to 1.8 V before powering up VBAT. Connect the test points as shown in **Figure 28** can manually force the module to enter download mode.



# 4 RF Specifications

The impedance of the antenna port is 50 Ω. The antenna interfaces of EG95 series are shown as follow:

- One main antenna interface
- One Rx-diversity antenna interface (which is used to resist the fall of signals caused by high speed movement and multipath effect)
- One GNSS antenna interface

## 4.1. Cellular Network

### 4.1.1. Antenna Interfaces & Frequency Bands

The pin definition of main antenna and Rx-diversity antenna interfaces is shown below.

**Table 23: Pin Definition of RF Antennas**

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN	60	AIO	Main antenna interface	50 Ω impedance
ANT_DIV (EG95-E) ANT_GNSS (EG95-NA/-EX/ -NAX/-NAXD/-AUX)	49	AI	Diversity antenna interface	50 Ω impedance. If unused, keep these pins open.
RESERVED (EG95-E) ANT_DIV (EG95-NA/-EX/ -NAX/-NAXD/-AUX)	56	AI	Diversity antenna interface	

### 4.1.2. Operating Frequency

**Table 24: Module Operating Frequencies**

3GPP Band	Transmit	Receive	Unit
GSM850	824–849	869–894	MHz
EGSM900	880–915	925–960	MHz
DCS1800	1710–1785	1805–1880	MHz
PCS1900	1850–1910	1930–1990	MHz
WCDMA B1	1920–1980	2110–2170	MHz
WCDMA B2	1850–1910	1930–1990	MHz
WCDMA B4	1710–1755	2110–2155	MHz
WCDMA B5	824–849	869–894	MHz
WCDMA B8	880–915	925–960	MHz
LTE-FDD B1	1920–1980	2110–2170	MHz
LTE-FDD B2	1850–1910	1930–1990	MHz
LTE-FDD B3	1710–1785	1805–1880	MHz
LTE-FDD B4	1710–1755	2110–2155	MHz
LTE-FDD B5	824–849	869–894	MHz
LTE-FDD B7	2500–2570	2620–2690	MHz
LTE-FDD B8	880–915	925–960	MHz
LTE-FDD B12	699–716	729–746	MHz
LTE-FDD B13	777–787	746–756	MHz
LTE-FDD B20	832–862	791–821	MHz
LTE-FDD B25	1850–1915	1930–1995	MHz
LTE-FDD B26	814–849	859–894	MHz
LTE-FDD B28	703–748	758–803	MHz

LTE-FDD B66	1710–1780	2110–2180	MHz
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### 4.1.3. Tx Power

The following table shows the Tx power of EG95 series module.

**Table 25: Tx Power**

Frequency	Max. Tx Power	Min. Tx Power
GSM850/EGSM900	33 dBm $\pm$ 2 dB	5 dBm $\pm$ 5 dB
DCS1800/PCS1900	30 dBm $\pm$ 2 dB	0 dBm $\pm$ 5 dB
GSM850/EGSM900 (8-PSK)	27 dBm $\pm$ 3 dB	5 dBm $\pm$ 5 dB
DCS1800/PCS1900 (8-PSK)	26 dBm $\pm$ 3 dB	0 dBm $\pm$ 5 dB
WCDMA B1/B2/B4/B5/B8	24 dBm +1/-3 dB	< -49 dBm
LTE-FDD B1/B2/B3/B4/B5/B7/B8/B12/B13/B20/B25/ B26/B28/B66	23 dBm $\pm$ 2 dB	< -39 dBm

**NOTE**

In GPRS 4 slots TX mode, the maximum output power is reduced by 3.0 dB. The design conforms to the GSM specification as described in **Chapter 13.16** of *3GPP TS 51.010-1*.

### 4.1.4. Rx Sensitivity

The following tables show the conducted RF receiving sensitivity of EG95 series module.

**Table 26: EG95-E Conducted RF Receiving Sensitivity**

Frequency	Primary	Diversity	SIMO	3GPP
EGSM900	-108.6 dBm	-	-	-102 dBm
DCS1800	-109.4 dBm	-	-	-102 dBm
WCDMA B1	-109.5 dBm	-110 dBm	-112.5 dBm	-106.7 dBm

WCDMA B8	-109.5 dBm	-110 dBm	-112.5 dBm	-103.7 dBm
LTE-FDD B1 (10 MHz)	-97.5 dBm	-98.3 dBm	-101.4 dBm	-96.3 dBm
LTE-FDD B3 (10 MHz)	-98.3 dBm	-98.5 dBm	-101.5 dBm	-93.3 dBm
LTE-FDD B7 (10 MHz)	-96.3 dBm	-98.4 dBm	-101.3 dBm	-94.3 dBm
LTE-FDD B8 (10 MHz)	-97.1 dBm	-99.1 dBm	-101.2 dBm	-93.3 dBm
LTE-FDD B20 (10 MHz)	-97 dBm	-99 dBm	-101.3 dBm	-93.3 dBm
LTE-FDD B28A (10 MHz)	-98.3 dBm	-99 dBm	-101.4 dBm	-94.8 dBm

**Table 27: EG95-NA Conducted RF Receiving Sensitivity**

Frequency	Primary	Diversity	SIMO	3GPP
WCDMA B2	-110 dBm	-110 dBm	-112.5 dBm	-104.7 dBm
WCDMA B4	-110 dBm	-110 dBm	-112.5 dBm	-106.7 dBm
WCDMA B5	-111 dBm	-111 dBm	-113 dBm	-104.7 dBm
LTE-FDD B2 (10 MHz)	-98 dBm	-99 dBm	-102.2 dBm	-94.3 dBm
LTE-FDD B4 (10 MHz)	-97.8 dBm	-99.5 dBm	-102.2 dBm	-96.3 dBm
LTE-FDD B5 (10 MHz)	-99.6 dBm	-100.3 dBm	-103 dBm	-94.3 dBm
LTE-FDD B12 (10 MHz)	-99.5 dBm	-100 dBm	-102.5 dBm	-93.3 dBm
LTE-FDD B13 (10 MHz)	-99.2 dBm	-100 dBm	-102.5 dBm	-93.3 dBm

**Table 28: EG95-EX Conducted RF Receiving Sensitivity**

Frequency	Primary	Diversity	SIMO	3GPP
EGSM900	-109.8 dBm	-	-	-102 dBm
DCS1800	-109.8 dBm	-	-	-102 dbm
WCDMA B1	-110 dBm	-111 dBm	-112.5 dBm	-106.7 dBm
WCDMA B8	-110 dBm	-111 dBm	-112.5 dBm	-103.7 dBm

LTE-FDD B1 (10 MHz)	-98.7 dBm	-98.8 dBm	-102.4 dBm	-96.3 dBm
LTE-FDD B3 (10 MHz)	-98.3 dBm	-99.5 dBm	-102.5 dBm	-93.3 dBm
LTE-FDD B7 (10 MHz)	-97.5 dBm	-98.4 dBm	-100.3 dBm	-94.3 dBm
LTE-FDD B8 (10 MHz)	-98.7 dBm	-99.6 dBm	-102.2 dBm	-93.3 dBm
LTE-FDD B20 (10 MHz)	-97 dBm	-97.5 dBm	-102.2 dBm	-93.3 dBm
LTE-FDD B28 (10 MHz)	-98.2 dBm	-99.5 dBm	-102 dBm	-94.8 dBm

**Table 29: EG95-NAX Conducted RF Receiving Sensitivity**

Frequency	Primary	Diversity	SIMO	3GPP
WCDMA B2	-110 dBm	-110 dBm	-112.5 dBm	-104.7 dBm
WCDMA B4	-110 dBm	-110 dBm	-112.5 dBm	-106.7 dBm
WCDMA B5	-111 dBm	-111 dBm	-113 dBm	-104.7 dBm
LTE-FDD B2 (10 MHz)	-98 dBm	-99 dBm	-102.2 dBm	-94.3 dBm
LTE-FDD B4 (10 MHz)	-97.8 dBm	-99.5 dBm	-102.2 dBm	-96.3 dBm
LTE-FDD B5 (10 MHz)	-99.4 dBm	-100 dBm	-102.7 dBm	-94.3 dBm
LTE-FDD B12 (10 MHz)	-99.5 dBm	-100 dBm	-102.5 dBm	-93.3 dBm
LTE-FDD B13 (10 MHz)	-99.2 dBm	-100 dBm	-102.5 dBm	-93.3 dBm
LTE-FDD B25 (10 MHz)	-97.6 dBm	-99 dBm	-102.2 dBm	-92.8 dBm
LTE-FDD B26 (10 MHz)	-99.1 dBm	-99.9 dBm	-102.7 dBm	-93.8 dBm

**Table 30: EG95-NAXD Conducted RF Receiving Sensitivity**

Frequency	Primary	Diversity	SIMO	3GPP
WCDMA B2	-110 dBm	-110 dBm	-112.5 dBm	-104.7 dBm
WCDMA B4	-110 dBm	-110 dBm	-112.5 dBm	-106.7 dBm
WCDMA B5	-111 dBm	-111 dBm	-113 dBm	-104.7 dBm

LTE-FDD B2 (10 MHz)	-98 dBm	-99 dBm	-102.2 dBm	-94.3 dBm
LTE-FDD B4 (10 MHz)	-97.8 dBm	-99.5 dBm	-102.2 dBm	-96.3 dBm
LTE-FDD B5 (10 MHz)	-99.4 dBm	-100 dBm	-102.7 dBm	-94.3 dBm
LTE-FDD B12 (10 MHz)	-99.5 dBm	-100 dBm	-102.5 dBm	-93.3 dBm
LTE-FDD B13 (10 MHz)	-99.2 dBm	-100 dBm	-102.5 dBm	-93.3 dBm
LTE-FDD B25 (10 MHz)	-97.6 dBm	-99 dBm	-102.2 dBm	-92.8 dBm
LTE-FDD B26 (10 MHz)	-99.1 dBm	-99.9 dBm	-102.7 dBm	-93.8 dBm

**Table 31: EG95-AUX Conducted RF Receiving Sensitivity**

Frequency	Primary	Diversity	SIMO	3GPP
GSM850	-109.1 dBm	-	-	-102 dBm
EGSM900	-109.7 dBm	-	-	-102 dBm
DCS1800	-110.0 dBm	-	-	-102 dBm
PCS1900	-109.4 dBm	-	-	-102 dBm
WCDMA B1	-109.2 dBm	-109.5 dBm	-	-106.7 dBm
WCDMA B2	-109.8 dBm	-111 dBm	-	-104.7 dBm
WCDMA B5	-110 dBm	-111 dBm	-	-104.7 dBm
WCDMA B8	-110 dBm	-111 dBm	-	-103.7 dBm
LTE-FDD B1 (10 MHz)	-97.2 dBm	-98.9 dBm	-101.2 dBm	-96.3 dBm
LTE-FDD B2 (10 MHz)	-97.7 dBm	-98.9 dBm	-101.7 dBm	-94.3 dBm
LTE-FDD B3 (10 MHz)	-98.2 dBm	-99.1 dBm	-102.2 dBm	-93.3 dBm
LTE-FDD B4 (10 MHz)	-97.7 dBm	-98.7 dBm	-101.2 dBm	-96.3 dBm
LTE-FDD B5 (10 MHz)	-99.2 dBm	-99.7 dBm	-102.7 dBm	-94.3 dBm
LTE-FDD B7 (10 MHz)	-96.7 dBm	-97.1 dBm	-99.7 dBm	-94.3 dBm
LTE-FDD B8 (10 MHz)	-98.0 dBm	-98.4 dBm	-102.2 dBm	-93.3 dBm

LTE-FDD B28 (10 MHz)	-98.7 dBm	-98.5 dBm	-101.7 dBm	-94.8 dBm
LTE-FDD B66 (10 MHz)	-97.7 dBm	-98.8 dBm	-101.2 dBm	-95.8 dBm

### 4.1.5. Reference Design

A reference design of ANT\_MAIN and ANT\_DIV antenna pads is shown as below. A  $\pi$ -type matching circuit should be reserved for better RF performance. The capacitors are not mounted by default. Place the  $\pi$ -type matching components (R1/C1/C2, R2/C3/C4) as close to the antenna as possible.

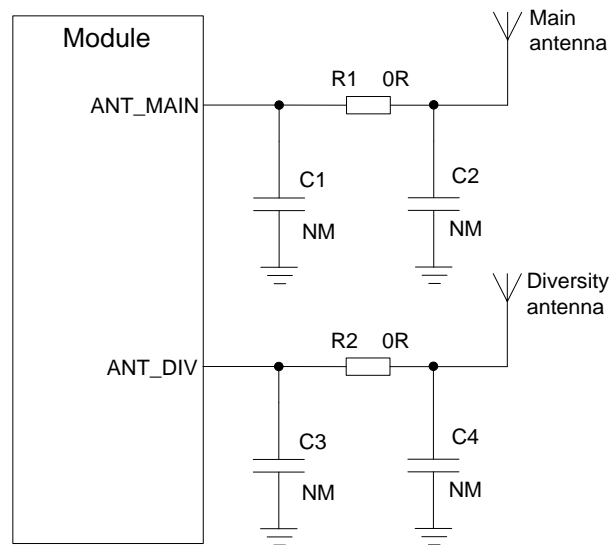


Figure 30: Reference Circuit of RF Antenna Interface

**NOTE**

1. Keep a proper distance between the main antenna and the Rx-diversity antenna to improve the receiving sensitivity.
2. For the operation of ANT\_MAIN and ANT\_DIV, see `AT+QCFG="divctl"` in *document [5]* for details.

## 4.2. GNSS

EG95 series module includes a fully integrated global navigation satellite system solution that supports GPS, GLONASS, BDS, Galileo and QZSS.

EG95 series module supports standard NMEA 0183 protocol, and outputs NMEA sentences at 1 Hz data update rate via USB interface by default.

By default, EG95 series module GNSS engine is switched off. It has to be switched on via AT command. For more details about GNSS engine technology and configurations, see **document [4]**.

**4.2.1. Antenna Interfaces & Frequency Bands**

The GNSS antenna interface is only supported on EG95-NA/-EX/-NAX/-NAXD/-AUX. The following tables show pin definition and frequency specification of GNSS antenna interface.

**Table 32: Pin Definition of GNSS Antenna Interface**

Pin Name	Pin No.	I/O	Description	Comment
ANT_GNSS (EG95-NA/-EX/-NAX/-NAXD/-AUX)	49	AI	GNSS antenna interface	50 Ω impedance

**Table 33: GNSS Frequency**

Type	Frequency	Unit
GPS	1575.42 ±1.023	MHz
GLONASS	1597.5–1605.8	MHz
Galileo	1575.42 ±2.046	MHz
BDS	1561.098 ±2.046	MHz
QZSS	1575.42	MHz

**4.2.2. GNSS Performance**

The following table shows GNSS performance of EG95 series module.

**Table 34: GNSS Performance**

Parameter	Description	Conditions	Typ.	Unit
Sensitivity (GNSS)	Acquisition	Autonomous	-146	dBm
	Reacquisition	Autonomous	-157	dBm
	Tracking	Autonomous	-157	dBm



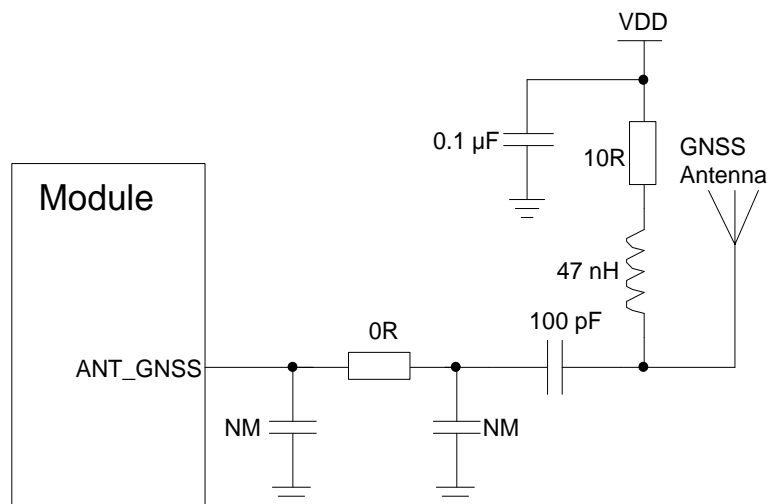
	Cold start @ open sky	Autonomous	34.6	s
		XTRA enabled	11.57	s
TTF (GNSS)	Warm start @ open sky	Autonomous	26.09	s
		XTRA enabled	3.7	s
	Hot start @ open sky	Autonomous	1.8	s
		XTRA enabled	3.4	s
Accuracy (GNSS)	CEP-50	Autonomous @ open sky	< 2.5	m

**NOTE**

1. Tracking sensitivity: the minimum GNSS signal power at which the module can maintain lock (keep positioning for at least 3 minutes continuously).
2. Reacquisition sensitivity: the minimum GNSS signal power required for the module to maintain lock within 3 minutes after loss of lock.
3. Acquisition sensitivity: the minimum GNSS signal power at which the module can fix position successfully within 3 minutes after executing cold start command.

**4.2.3. Reference Design**

A reference design of GNSS antenna is shown as below.



**Figure 31: Reference Circuit of GNSS Antenna**

**NOTE**

1. An external LDO can be selected to supply power according to the active antenna requirement.
2. If the module is designed with a passive antenna, then the VDD circuit is not needed.

**4.2.4. Layout Guidelines**

The following layout guidelines should be taken into account in your design.

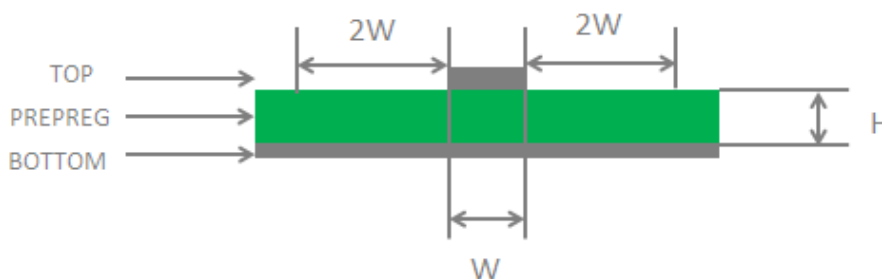
- Maximize the distance among GNSS antenna, main antenna and Rx-diversity antenna.
- Digital circuits such as (U)SIM card, USB interface, camera module and display connector should be kept away from the antennas.
- Use ground vias around the GNSS trace and sensitive analog signal traces to provide coplanar isolation and protection.
- Keep the characteristic impedance for ANT\_GNSS trace as 50 Ω.

**NOTE**

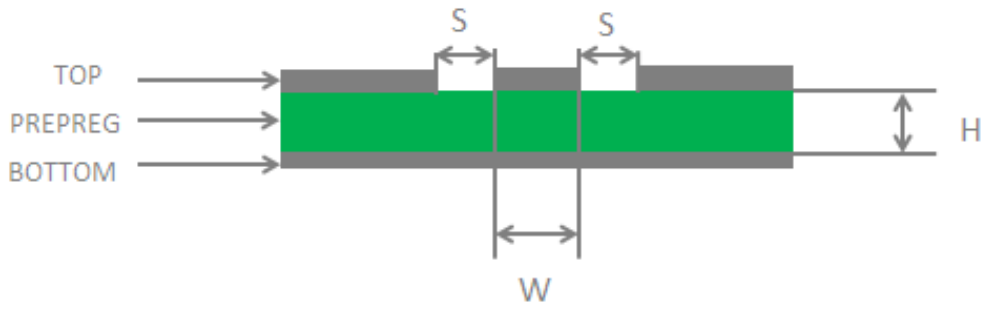
It is recommended to use a passive antenna. If active antennas are required, it is strongly recommended to reserve a  $\pi$ -type attenuation and ensure that the total gain of the external GNSS RF path of the module is not greater than 0 dB. At the same time, this may compromise the GNSS performance, depending on the performance of the active antenna.

**4.3. RF Routing Guidelines**

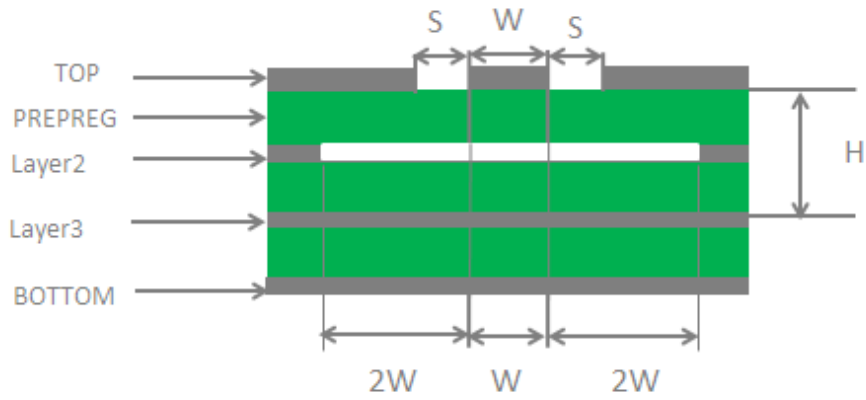
For user’s PCB, the characteristic impedance of all RF traces should be controlled to 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials’ dielectric constant, the height from the reference ground to the signal layer (H), and the spacing between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.



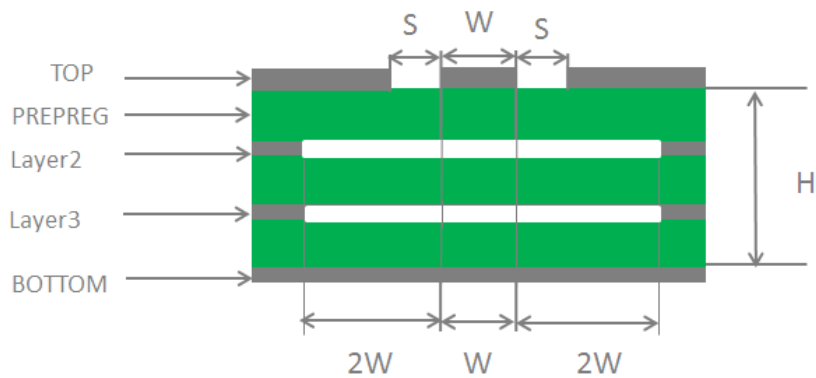
**Figure 32: Microstrip Design on a 2-layer PCB**



**Figure 33: Coplanar Waveguide Design on a 2-layer PCB**



**Figure 34: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)**



**Figure 35: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)**

To ensure RF performance and reliability, the following principles should be complied with in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible, and all the right-angle traces should be changed to curved ones. The recommended trace angle is 135°.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be no less than two times the width of RF signal traces (2 × W).
- Keep RF traces away from interference sources, and avoid intersection and paralleling between traces on adjacent layers.

For more details about RF layout, see **document [6]**.

#### 4.4. Antenna Design Requirements

The following table shows the requirements on main antenna, Rx-diversity antenna and GNSS antenna.

**Table 35: Antenna Design Requirements**

Type	Requirements
GNSS <sup>9</sup>	Frequency range: 1559–1609 MHz Polarization: RHCP or linear VSWR: < 2 (Typ.) Passive antenna gain: > 0 dBi Active antenna noise figure: < 1.5 dB Active antenna gain: > 0 dBi Active antenna embedded LNA gain: < 17 dB
GSM/WCDMA/LTE	VSWR: ≤ 2 Efficiency: > 30 % Max. input power: 50 W Input impedance: 50 Ω Cable insertion loss: <b>&lt; 1 dB: LB (&lt;1 GHz)</b>

<sup>9</sup> It is recommended to use a passive GNSS antenna when LTE B13 is supported, as the use of active antenna may generate harmonics which will affect the GNSS performance.

< 1.5 dB: MB (1–2.3 GHz)  
 < 2 dB: HB (> 2.3 GHz)

### 4.5. RF Connector Recommendation

If RF connector is used for antenna connection, it is recommended to use U.FL-R-SMT connector provided by Hirose.

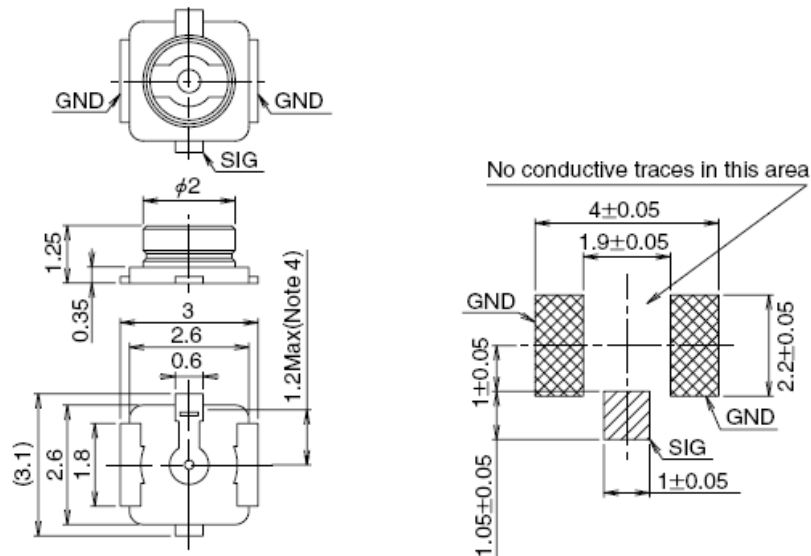


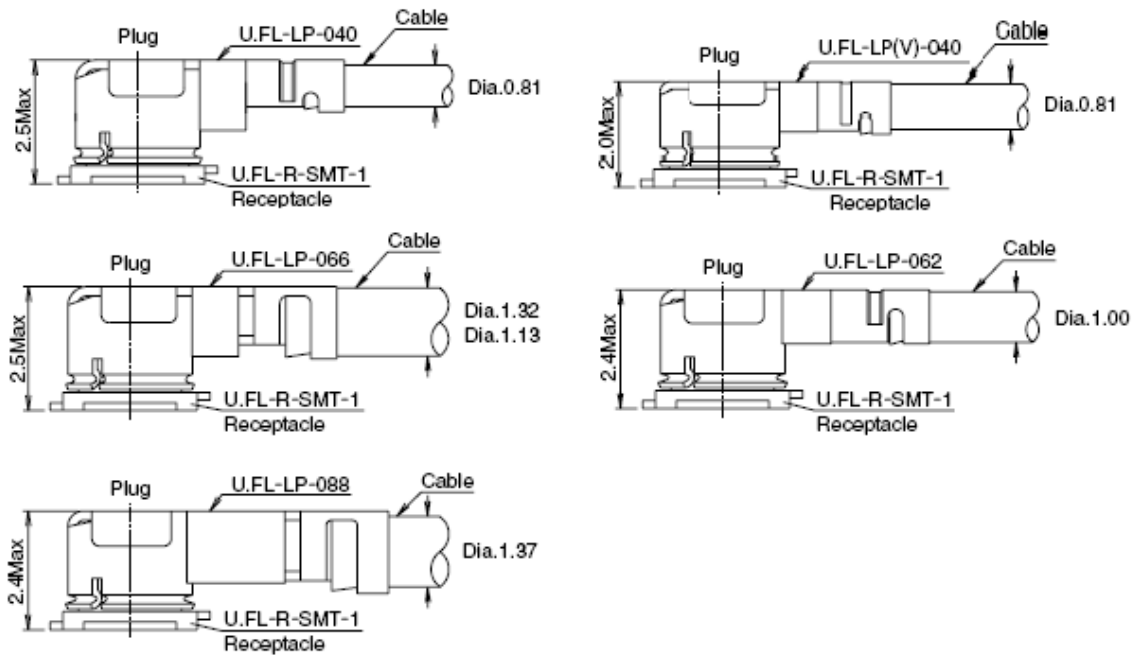
Figure 36: Dimensions of the Receptacle (Unit: mm)

U.FL-LP series mated plugs listed in the following figure can be used to match the U.FL-R-SMT.

	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
Part No.					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 37: Specifications of Mated Plugs

The following figure describes the space factor of mated connector.



**Figure 38: Space Factor of Mated Connectors (Unit: mm)**

For more details, visit <http://www.hirose.com>.

# 5 Electrical Characteristics and Reliability

## 5.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

**Table 36: Absolute Maximum Ratings**

Parameter	Min.	Max.	Unit
VBAT_RF/VBAT_BB	-0.3	4.7	V
USB_VBUS	-0.3	5.5	V
Peak Current of VBAT_BB	-	0.8	A
Peak Current of VBAT_RF	-	1.8	A
Voltage at Digital Pins	-0.3	2.3	V
ADC0	0	VBAT_BB	V

## 5.2. Power Supply Ratings

**Table 37: Power Supply Ratings**

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
VBAT	VBAT_BB and VBAT_RF	The actual input voltages must be kept between the minimum and maximum values.	3.3	3.8	4.3	V

	Voltage drop during burst transmission	Maximum power control level on EGSM900	-	-	400	mV
I <sub>VBAT</sub>	Peak supply current (during transmission slot)	Maximum power control level on EGSM900	-	1.8	2.0	A
USB_VBUS	USB connection detection	-	3.0	5.0	5.25	V

### 5.3. Operating and Storage Temperatures

The operating and storage temperatures are listed in the following table.

**Table 38: Operating and Storage Temperatures**

Parameter	Min.	Typ.	Max.	Unit
Operating Temperature Range <sup>10</sup>	-35	+25	+75	°C
Extended Temperature Range <sup>11</sup>	-40	-	+85	°C
Storage Temperature Range	-40	-	+90	°C

### 5.4. Power Consumption

**Table 39: EG95-E Power Consumption**

Description	Conditions	Typ.	Unit
OFF state	Power down	15	µA
Sleep state	<b>AT+CFUN=0</b> (USB disconnected)	1.3	mA
	EGSM900 DRX = 2 (USB disconnected)	2.3	mA

<sup>10</sup> Within the operating temperature range, the module meets 3GPP specifications.

<sup>11</sup> Within the extended temperature range, the module remains the ability to establish and maintain functions such as voice, SMS, data transmission, etc., without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as P<sub>out</sub>, may exceed the specified tolerances of 3GPP. When the temperature returns to the operating temperature range, the module meets 3GPP specifications again.



	EGSM900 DRX = 5 (USB suspended)	2.0	mA
	EGSM900 DRX = 9 (USB disconnected)	1.6	mA
	WCDMA PF = 64 (USB disconnected)	1.8	mA
	WCDMA PF = 64 (USB suspended)	2.1	mA
	WCDMA PF = 512 (USB disconnected)	1.3	mA
	LTE-FDD PF = 64 (USB disconnected)	2.3	mA
	LTE-FDD PF = 64 (USB suspended)	2.6	mA
	LTE-FDD PF = 256 (USB disconnected)	1.5	mA
Idle state	EGSM900 DRX = 5 (USB disconnected)	21.0	mA
	EGSM900 DRX = 5 (USB connected)	31.0	mA
	WCDMA PF = 64 (USB disconnected)	21.0	mA
	WCDMA PF = 64 (USB connected)	31.0	mA
	LTE-FDD PF = 64 (USB disconnected)	21.0	mA
	LTE-FDD PF = 64 (USB connected)	31.0	mA
GPRS data transfer	EGSM900 4DL/1UL @ 32.35 dBm	268	mA
	EGSM900 3DL/2UL @ 32.16 dBm	459	mA
	EGSM900 2DL/3UL @ 30.57 dBm	547	mA
	EGSM900 1DL/4UL @ 29.45 dBm	631	mA
	DCS1800 4DL/1UL @ 29.14 dBm	177	mA
	DCS1800 3DL/2UL @ 29.07 dBm	290	mA
	DCS1800 2DL/3UL @ 28.97 dBm	406	mA
	DCS1800 1DL/4UL @ 28.88 dBm	517	mA
EDGE data transfer	EGSM900 4DL/1UL PCL = 8 @ 26.88 dBm	167	mA
	EGSM900 3DL/2UL PCL = 8 @ 26.84 dBm	278	mA
	EGSM900 2DL/3UL PCL = 8 @ 26.76 dBm	385	mA

	EGSM900 1DL/4UL PCL = 8 @ 26.54 dBm	492	mA
	DCS1800 4DL/1UL PCL = 2 @ 25.66 dBm	169	mA
	DCS1800 3DL/2UL PCL = 2 @ 25.59 dBm	256	mA
	DCS1800 2DL/3UL PCL = 2 @ 25.51 dBm	341	mA
	DCS1800 1DL/4UL PCL = 2 @ 25.38 dBm	432	mA
WCDMA data transfer	WCDMA B1 HSDPA @ 22.48 dBm	586	mA
	WCDMA B1 HSUPA @ 22.29 dBm	591	mA
	WCDMA B8 HSDPA @ 22.24 dBm	498	mA
	WCDMA B8 HSUPA @ 21.99 dBm	511	mA
LTE data transfer	LTE-FDD B1 @ 23.37 dBm	736	mA
	LTE-FDD B3 @ 22.97 dBm	710	mA
	LTE-FDD B7 @ 23.17 dBm	775	mA
	LTE-FDD B8 @ 23.04 dBm	651	mA
	LTE-FDD B20 @ 23.21 dBm	699	mA
	LTE-FDD B28A @ 22.76 dBm	714	mA
GSM voice call	EGSM900 PCL = 5 @ 32.36 dBm	271	mA
	DCS1800 PCL = 0 @ 29.19 dBm	181	mA
WCDMA voice call	WCDMA B1 @ 22.91 dBm	632	mA
	WCDMA B8 @ 23.14 dBm	546	mA

**Table 40: EG95-NA Power Consumption**

Description	Conditions	Typ.	Unit
OFF state	Power down	13	μA
Sleep state	<b>AT+CFUN=0</b> (USB disconnected)	1.0	mA
	WCDMA PF = 64 (USB disconnected)	2.2	mA

	WCDMA PF = 64 (USB suspended)	2.5	mA
	WCDMA PF = 512 (USB disconnected)	1.4	mA
	LTE-FDD PF = 64 (USB disconnected)	2.6	mA
	LTE-FDD PF = 64 (USB suspended)	2.9	mA
	LTE-FDD PF = 256 (USB disconnected)	1.7	mA
Idle state	WCDMA PF = 64 (USB disconnected)	14.0	mA
	WCDMA PF = 64 (USB connected)	26.0	mA
	LTE-FDD PF = 64 (USB disconnected)	15.0	mA
	LTE-FDD PF = 64 (USB connected)	26.0	mA
WCDMA data transfer	WCDMA B2 HSDPA CH9938 @ 22.45 dBm	569	mA
	WCDMA B2 HSUPA CH9938 @ 21.73 dBm	559	mA
	WCDMA B4 HSDPA CH1537 @ 23.05 dBm	572	mA
	WCDMA B4 HSUPA CH1537 @ 22.86 dBm	586	mA
	WCDMA B5 HSDPA CH4407 @ 23 dBm	518	mA
	WCDMA B5 HSUPA CH4407 @ 22.88 dBm	514	mA
LTE data transfer	LTE-FDD B2 CH1100 @ 23.29 dBm	705	mA
	LTE-FDD B4 CH2175 @ 23.19 dBm	693	mA
	LTE-FDD B5 CH2525 @ 23.39 dBm	601	mA
	LTE-FDD B12 CH5060 @ 23.16 dBm	650	mA
	LTE-FDD B13 CH5230 @ 23.36 dBm	602	mA
WCDMA voice call	WCDMA B2 CH9938 @ 23.34 dBm	627	mA
	WCDMA B4 CH1537 @ 23.47 dBm	591	mA
	WCDMA B5 CH4357 @ 23.37 dBm	536	mA

Table 41: EG95-EX Power Consumption

Description	Conditions	Typ.	Unit
OFF state	Power down	15	μA
Sleep state	<b>AT+CFUN=0</b> (USB disconnected)	1.3	mA
	EGSM900 DRX = 2 (USB disconnected)	2.3	mA
	EGSM900 DRX = 5 (USB suspend)	2.0	mA
	EGSM900 DRX = 9 (USB disconnected)	1.6	mA
	WCDMA PF = 64 (USB disconnected)	1.8	mA
	WCDMA PF = 64 (USB suspend)	2.1	mA
	WCDMA PF = 512 (USB disconnected)	1.3	mA
	LTE-FDD PF = 64 (USB disconnected)	2.3	mA
	LTE-FDD PF = 64 (USB suspend)	2.6	mA
	LTE-FDD PF = 256 (USB disconnected)	1.5	mA
Idle state	EGSM900 DRX = 5 (USB disconnected)	21.0	mA
	EGSM900 DRX = 5 (USB connected)	31.0	mA
	WCDMA PF = 64 (USB disconnected)	21.0	mA
	WCDMA PF = 64 (USB connected)	31.0	mA
	LTE-FDD PF = 64 (USB disconnected)	21.0	mA
	LTE-FDD PF = 64 (USB connected)	31.0	mA
GPRS data transfer	EGSM900 4DL/1UL @ 33.06 dBm	247.9	mA
	EGSM900 3DL/2UL @ 32.93 dBm	450.8	mA
	EGSM900 2DL/3UL @ 31.1 dBm	536.4	mA
	EGSM900 1DL/4UL @ 29.78 dBm	618	mA
	DCS1800 4DL/1UL @ 29.3 dBm	144	mA
	DCS1800 3DL/2UL @ 29.3 dBm	253.4	mA

	DCS1800 2DL/3UL @ 29.21 dBm	355.4	mA
	DCS1800 1DL/4UL @ 29.07 dBm	455.7	mA
EDGE data transfer	EGSM900 4DL/1UL PCL = 8 @ 27.29 dBm	169.5	mA
	EGSM900 3DL/2UL PCL = 8 @ 27.01 dBm	305.06	mA
	EGSM900 2DL/3UL PCL = 8 @ 26.86 dBm	434	mA
	EGSM900 1DL/4UL PCL = 8 @ 25.95 dBm	548	mA
	DCS1800 4DL/1UL PCL = 2 @ 26.11 dBm	135	mA
	DCS1800 3DL/2UL PCL = 2 @ 25.8 dBm	244	mA
	DCS1800 2DL/3UL PCL = 2 @ 25.7 dBm	349	mA
	DCS1800 1DL/4UL PCL = 2 @ 25.6 dBm	455	mA
	WCDMA data transfer	WCDMA B1 HSDPA @ 22.48 dBm	485
WCDMA B1 HSUPA @ 21.9 dBm		458	mA
WCDMA B8 HSDPA @ 22.6 dBm		556	mA
WCDMA B8 HSUPA @ 22.02 dBm		520	mA
LTE data transfer	LTE-FDD B1 @ 23.37 dBm	605	mA
	LTE-FDD B3 @ 23.3 dBm	667	mA
	LTE-FDD B7 @ 23.2 dBm	783	mA
	LTE-FDD B8 @ 23.09 dBm	637	mA
	LTE-FDD B20 @ 23.21 dBm	646	mA
	LTE-FDD B28 @ 22.76 dBm	661	mA
GSM voice call	EGSM900 PCL = 5 @ 32.36 dBm	259	mA
	DCS1800 PCL = 0 @ 29.5 dBm	149	mA
WCDMA voice call	WCDMA B1 @ 23.4 dBm	494	mA
	WCDMA B8 @ 23.6 dBm	608	mA

Table 42: EG95-NAX Power Consumption

Description	Conditions	Typ.	Unit
OFF state	Power down	11	μA
	<b>AT+CFUN=0</b> (USB disconnected)	1.1	mA
	WCDMA PF = 64 (USB disconnected)	2.0	mA
	WCDMA PF = 64 (USB suspend)	2.4	mA
Sleep state	WCDMA PF = 512 (USB disconnected)	1.5	mA
	LTE-FDD PF = 64 (USB disconnected)	2.6	mA
	LTE-FDD PF = 64 (USB suspend)	2.8	mA
	LTE-FDD PF = 256 (USB disconnected)	1.8	mA
	WCDMA PF = 64 (USB disconnected)	17.4	mA
Idle state	WCDMA PF = 64 (USB connected)	34.3	mA
	LTE-FDD PF = 64 (USB disconnected)	17.8	mA
	LTE-FDD PF = 64 (USB connected)	34.7	mA
	WCDMA B2 HSDPA @ 21.64 dBm	547	mA
	WCDMA B2 HSUPA @ 21.13 dBm	543	mA
WCDMA data transfer	WCDMA B4 HSDPA @ 22.15 dBm	554	mA
	WCDMA B4 HSUPA @ 22.21 dBm	541	mA
	WCDMA B5 HSDPA @ 22.39 dBm	502	mA
	WCDMA B5 HSUPA @ 22.12 dBm	509	mA
	LTE-FDD B2 @ 23.07 dBm	691	mA
	LTE-FDD B4 @ 23.09 dBm	713	mA
LTE data transfer	LTE-FDD B5 @ 23.31 dBm	580	mA
	LTE-FDD B12 @ 23.30 dBm	627	mA
	LTE-FDD B13 @ 23.32 dBm	619	mA

	LTE-FDD B25 @ 23.03 dBm	693	mA
	LTE-FDD B26 @ 22.97 dBm	628	mA
WCDMA voice call	WCDMA B2 @ 22.89 dBm	591	mA
	WCDMA B4 @ 22.76 dBm	577	mA
	WCDMA B5 @ 23.03 dBm	516	mA

**Table 43: EG95-NAXD Power Consumption**

Description	Conditions	Typ.	Unit
OFF state	Power down	11	μA
Sleep state	<b>AT+CFUN=0</b> (USB disconnected)	1.1	mA
	WCDMA PF = 64 (USB disconnected)	2.0	mA
	WCDMA PF = 64 (USB suspend)	2.4	mA
	WCDMA PF = 512 (USB disconnected)	1.5	mA
	LTE-FDD PF = 64 (USB disconnected)	2.6	mA
	LTE-FDD PF = 64 (USB suspend)	2.8	mA
	LTE-FDD PF = 256 (USB disconnected)	1.8	mA
Idle state	WCDMA PF = 64 (USB disconnected)	18	mA
	WCDMA PF = 64 (USB connected)	35	mA
	LTE-FDD PF = 64 (USB disconnected)	18	mA
	LTE-FDD PF = 64 (USB connected)	35	mA
WCDMA data transfer	WCDMA B2 HSDPA @ 21.64 dBm	547	mA
	WCDMA B2 HSUPA @ 21.13 dBm	543	mA
	WCDMA B4 HSDPA @ 22.15 dBm	554	mA
	WCDMA B4 HSUPA @ 22.21 dBm	541	mA
	WCDMA B5 HSDPA @ 22.39 dBm	502	mA

	WCDMA B5 HSUPA @ 22.12 dBm	509	mA
	LTE-FDD B2 @ 23.07 dBm	691	mA
	LTE-FDD B4 @ 23.09 dBm	713	mA
	LTE-FDD B5 @ 23.31 dBm	580	mA
LTE data transfer	LTE-FDD B12 @ 23.30 dBm	627	mA
	LTE-FDD B13 @ 23.32 dBm	619	mA
	LTE-FDD B25 @ 23.03 dBm	693	mA
	LTE-FDD B26 @ 22.97 dBm	628	mA

**Table 44: EG95-AUX Power Consumption**

Description	Conditions	Typ.	Unit
OFF state	Power down	10	μA
Sleep state	<b>AT+CFUN=0</b> (USB disconnected)	1.0	mA
	GSM850 DRX = 2 (USB disconnected)	1.9	mA
	GSM850 DRX = 5 (USB suspend)	1.4	mA
	GSM850 DRX = 9 (USB disconnected)	1.3	mA
	WCDMA PF = 64 (USB disconnected)	1.7	mA
	WCDMA PF = 64 (USB suspend)	1.9	mA
	WCDMA PF = 512 (USB disconnected)	1.1	mA
	LTE-FDD PF = 64 (USB disconnected)	2.2	mA
	LTE-FDD PF = 64 (USB suspend)	2.4	mA
	LTE-FDD PF = 256 (USB disconnected)	1.5	mA
Idle state	GSM850 DRX = 5 (USB disconnected)	15	mA
	GSM850 DRX = 5 (USB connected)	25	mA
	WCDMA PF = 64 (USB disconnected)	15	mA



	WCDMA PF = 64 (USB connected)	25	mA
	LTE-FDD PF = 64 (USB disconnected)	16	mA
	LTE-FDD PF = 64 (USB connected)	26	mA
GPRS data transfer	GSM850 4DL/1UL @ 32.48 dBm	217.9	mA
	GSM850 3DL/2UL @ 31.89dBm	372.3	mA
	GSM850 2DL/3UL @ 29.45 dBm	432.9	mA
	GSM850 1DL/4UL @ 28.31 dBm	513.9	mA
	EGSM900 4DL/1UL @ 33.17 dBm	235.1	mA
	EGSM900 3DL/2UL @ 32.16 dBm	387.7	mA
	EGSM900 2DL/3UL @ 29.77 dBm	446.5	mA
	EGSM900 1DL/4UL @ 28.59 dBm	540.0	mA
	DCS1800 4DL/1UL @ 30.19 dBm	154.4	mA
	DCS1800 3DL/2UL @ 29.23 dBm	258.0	mA
	DCS1800 2DL/3UL @ 27.19 dBm	332.4	mA
	DCS1800 1DL/4UL @ 26.14 dBm	419.1	mA
	PCS1900 4DL/1UL @ 30.22 dBm	155.0	mA
	PCS1900 3DL/2UL @ 29.48 dBm	259.5	mA
	PCS1900 2DL/3UL @ 27.50 dBm	333.1	mA
	PCS1900 1DL/4UL @ 26.44 dBm	416.8	mA
EDGE data transfer	GSM850 4DL/1UL PCL = 8 @ 25.75 dBm	161.8	mA
	GSM850 3DL/2UL PCL = 8 @ 25.49 dBm	291.8	mA
	GSM850 2DL/3UL PCL = 8 @ 23.26 dBm	410.2	mA
	GSM850 1DL/4UL PCL = 8 @ 22.01 dBm	520.5	mA
	EGSM900 4DL/1UL PCL = 8 @ 26.04 dBm	161.5	mA
	EGSM900 3DL/2UL PCL = 8 @ 25.86 dBm	294.6	mA

	EGSM900 2DL/3UL PCL = 8 @ 23.62 dBm	411.4	mA
	EGSM900 1DL/4UL PCL = 8 @ 22.27 dBm	520.8	mA
	DCS1800 4DL/1UL PCL = 2 @ 26.12 dBm	139.4	mA
	DCS1800 3DL/2UL PCL = 2 @ 25.02 dBm	250.7	mA
	DCS1800 2DL/3UL PCL = 2 @ 22.75 dBm	355.3	mA
	DCS1800 1DL/4UL PCL = 2 @ 21.47 dBm	452.1	mA
	PCS1900 4DL/1UL PCL = 2 @ 26.36 dBm	138.3	mA
	PCS1900 3DL/2UL PCL = 2 @ 25.2 dBm	248.2	mA
	PCS1900 2DL/3UL PCL = 2 @ 22.94 dBm	351.5	mA
	PCS1900 1DL/4UL PCL = 2 @ 21.67 dBm	448.8	mA
WCDMA data transfer	WCDMA B1 HSDPA @ 22.30 dBm	609.6	mA
	WCDMA B1 HSUPA @ 21.50 dBm	640.5	mA
	WCDMA B2 HSDPA @ 22.14 dBm	557.4	mA
	WCDMA B2 HSUPA @ 21.18 dBm	539.4	mA
	WCDMA B5 HSDPA @ 22.6 dBm	588.2	mA
	WCDMA B5 HSUPA @ 21.45 dBm	545.2	mA
	WCDMA B8 HSDPA @ 21.92 dBm	578.1	mA
	WCDMA B8 HSUPA @ 21.93 dBm	592.5	mA
LTE data transfer	LTE-FDD B1 @ 22.96 dBm	777.4	mA
	LTE-FDD B2 @ 22.79 dBm	634.4	mA
	LTE-FDD B3 @ 23.09 dBm	697.9	mA
	LTE-FDD B4 @ 22.83 dBm	704.6	mA
	LTE-FDD B5 @ 23.05 dBm	657.1	mA
	LTE-FDD B7 @ 22.71 dBm	765.3	mA
	LTE-FDD B8 @ 22.80 dBm	635.3	mA

	LTE-FDD B28 @ 22.84 dBm	670.0	mA
	LTE-FDD B66 @ 22.73 dBm	725.9	mA
GSM voice call	GSM850 PCL5 @ 32.57 dBm	227.8	mA
	EGSM900 PCL5 @ 33.21 dBm	253.8	mA
	DCS1800 PCL0 @ 30.24 dBm	168.0	mA
	PCS1900 PCL0 @ 30.33 dBm	166.8	mA
WCDMA voice call	WCDMA B1 @ 22.93 dBm	656.2	mA
	WCDMA B2 @ 22.95 dBm	579.8	mA
	WCDMA B5 @ 22.54 dBm	589.8	mA
	WCDMA B8 @ 22.47 dBm	627.8	mA

**Table 45: GNSS Power Consumption of EG95 Series Module**

Description	Conditions	Typ.	Unit
Searching (AT+CFUN=0)	Cold start @ Passive antenna	54	mA
	Hot start @ Passive antenna	54	mA
	Lost state @ Passive antenna	53	mA
Tracking (AT+CFUN=0)	Open sky @ Passive antenna	32	mA

## 5.5. ESD Protection

Static electricity occurs naturally and it may damage the module. Therefore, applying proper ESD countermeasures and handling methods is imperative. For example, wear anti-static gloves during the development, production, assembly and testing of the module; add ESD protection components to the ESD sensitive interfaces and points in the product design.

The following table shows the module’s electrostatic discharge characteristics.

**Table 46: Electrostatic Discharge Characteristics (25 °C, Humidity: 45 %)**

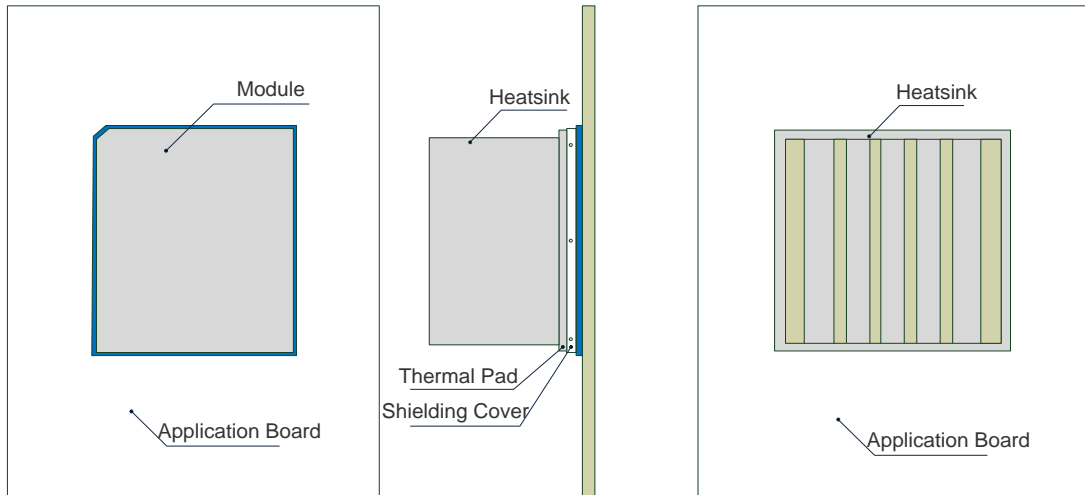
Tested Interfaces	Contact Discharge	Air Discharge	Unit
VBAT, GND	±5	±10	kV
All Antenna Interfaces	±4	±8	kV
Other Interfaces	±0.5	±1	kV

## 5.6. Thermal Dissipation

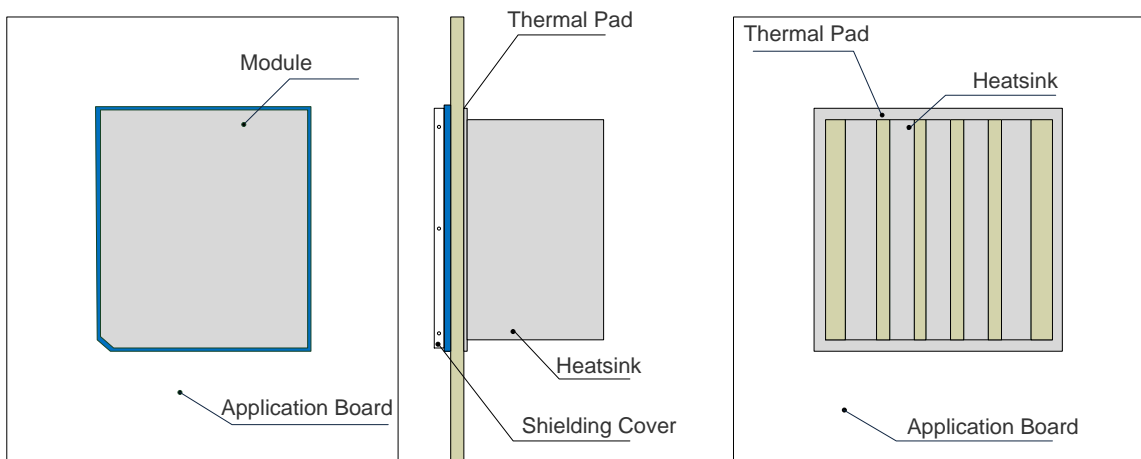
In order to achieve better performance of the module, it is recommended to comply with the following principles for thermal consideration:

- On your PCB design, please keep placement of the module away from heating sources, especially high power components such as ARM processor, audio power amplifier, power supply, etc.
- Do not place components on the opposite side of the PCB area where the module is mounted, in order to facilitate adding of heatsink when necessary.
- Do not apply solder mask on the opposite side of the PCB area where the module is mounted, so as to ensure better heat dissipation performance.
- The reference ground of the area where the module is mounted should be complete, and add ground vias as many as possible for better heat dissipation.
- Make sure the ground pads of the module and PCB are fully connected.
- According to your application demands, the heatsink can be mounted on the top of the module, or the opposite side of the PCB area where the module is mounted, or both of them.
- The heatsink should be designed with as many fins as possible to increase heat dissipation area. Meanwhile, a thermal pad with high thermal conductivity should be used between the heatsink and module/PCB.

The following shows two kinds of heatsink designs for reference and you can choose one or both of them according to their application structure.



**Figure 39: Referenced Heatsink Design (Heatsink at the Top of the Module)**



**Figure 40: Referenced Heatsink Design (Heatsink at the Backside of Customers' PCB)**

**NOTE**

1. The module offers the best performance when the internal BB chip stays below 105 °C. When the maximum temperature of the BB chip reaches or exceeds 105 °C, the module works normal but provides reduced performance (such as RF output power, data rate, etc.). When the maximum BB chip temperature reaches or exceeds 115 °C, the module will disconnect from the network, and it will recover to network connected state after the maximum temperature falls below 115 °C. Therefore, the thermal design should be maximally optimized to make sure the maximum BB chip temperature always maintains below 105 °C. You can execute **AT+QTEMP** and get the maximum BB chip temperature from the first returned value.
2. For more details about thermal design, see *document [7]*.

# 6 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are  $\pm 0.2$  mm unless otherwise specified.

## 6.1. Mechanical Dimensions

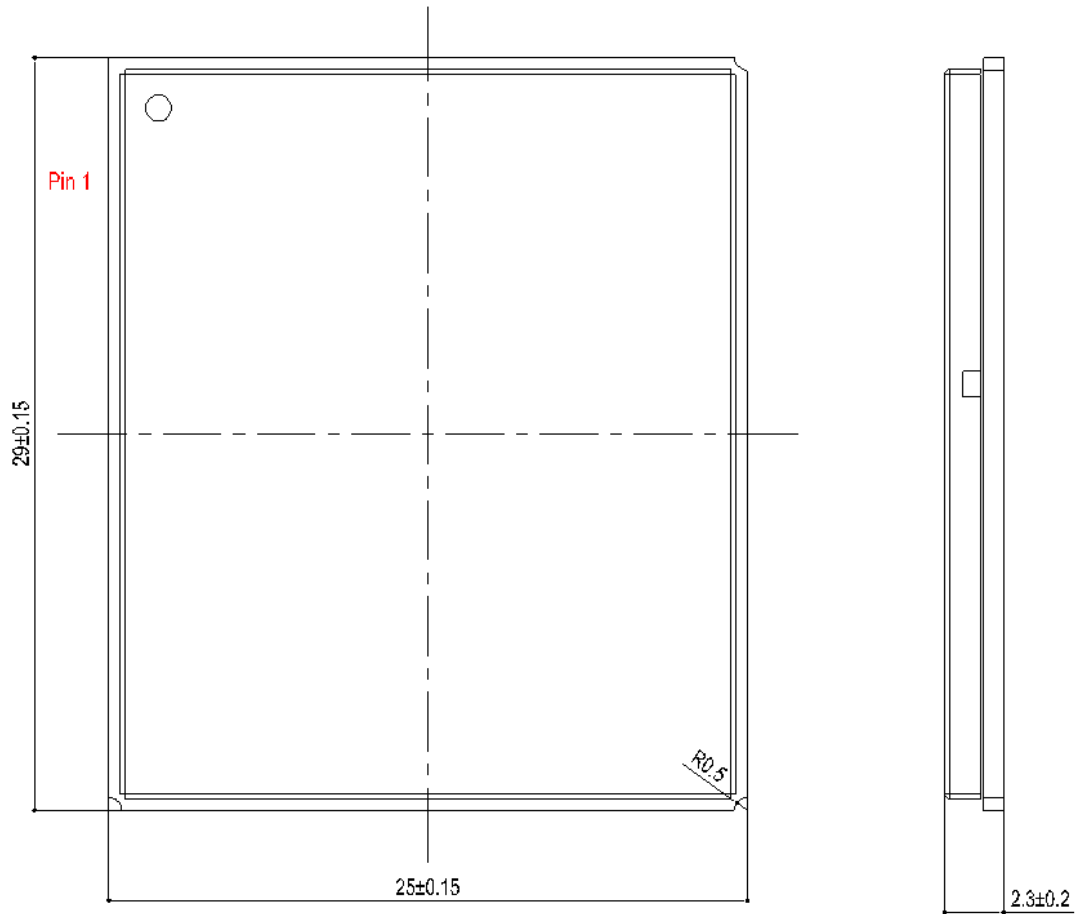


Figure 41: EG95-E Top and Side Dimensions

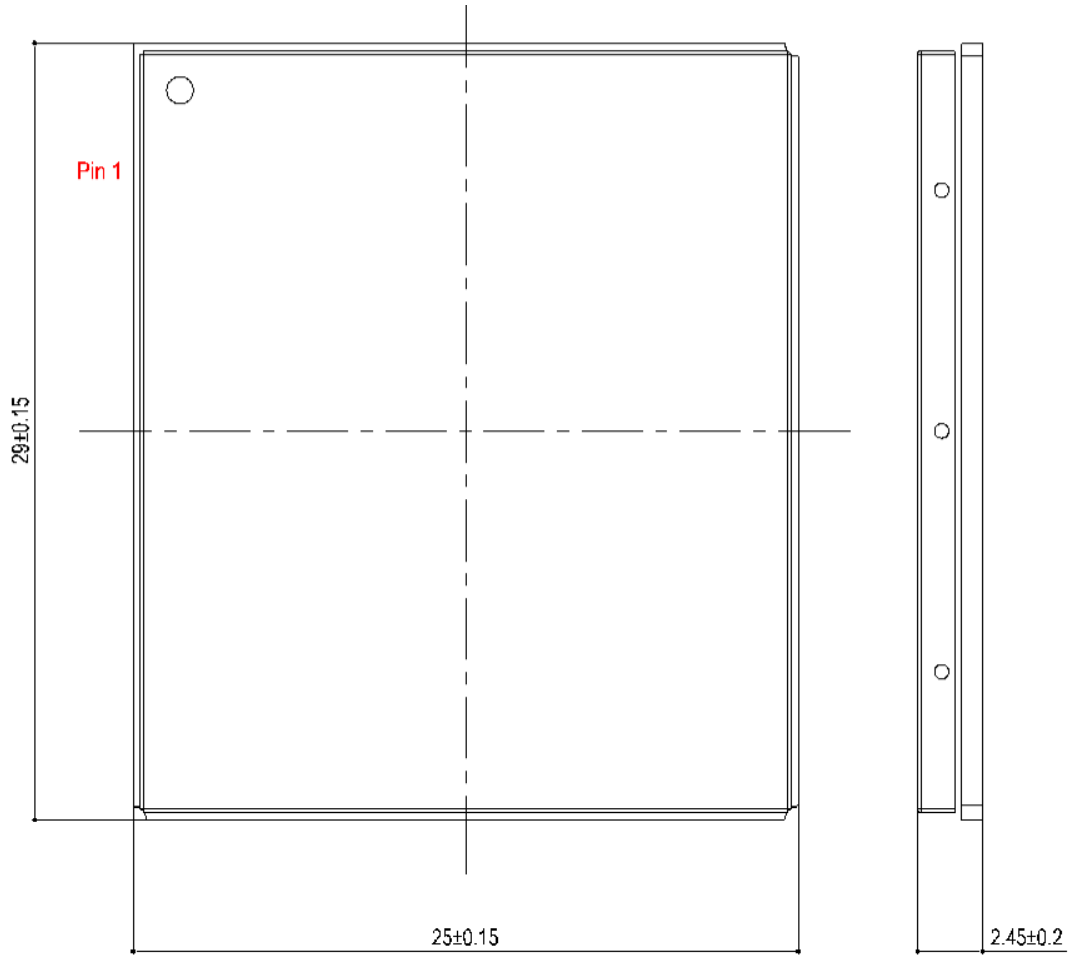


Figure 42: EG95-NA/-EX/-NAX/-NAXD/-AUX Top and Side Dimensions

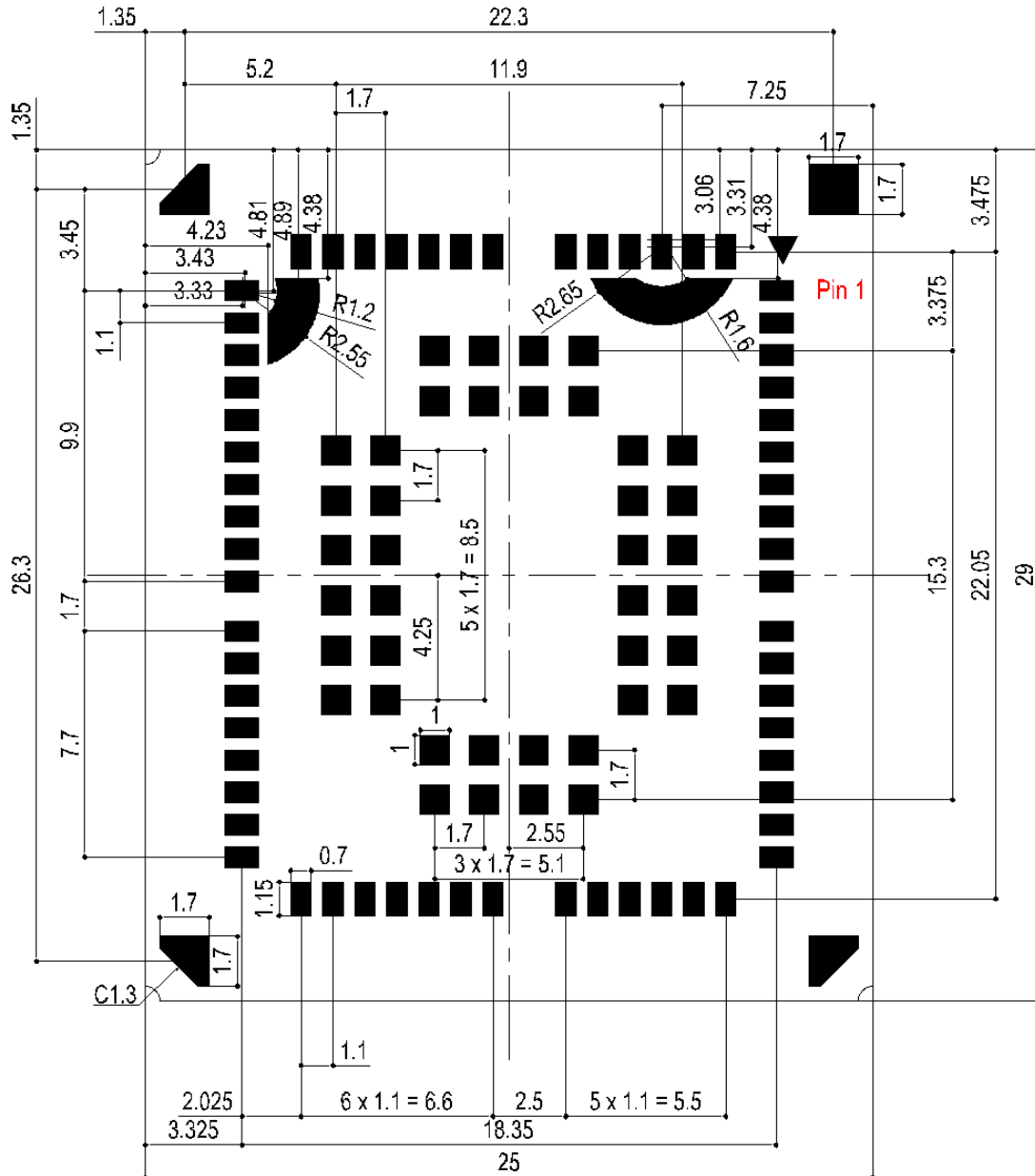


Figure 43: EG95-E Bottom Dimensions (Top View)



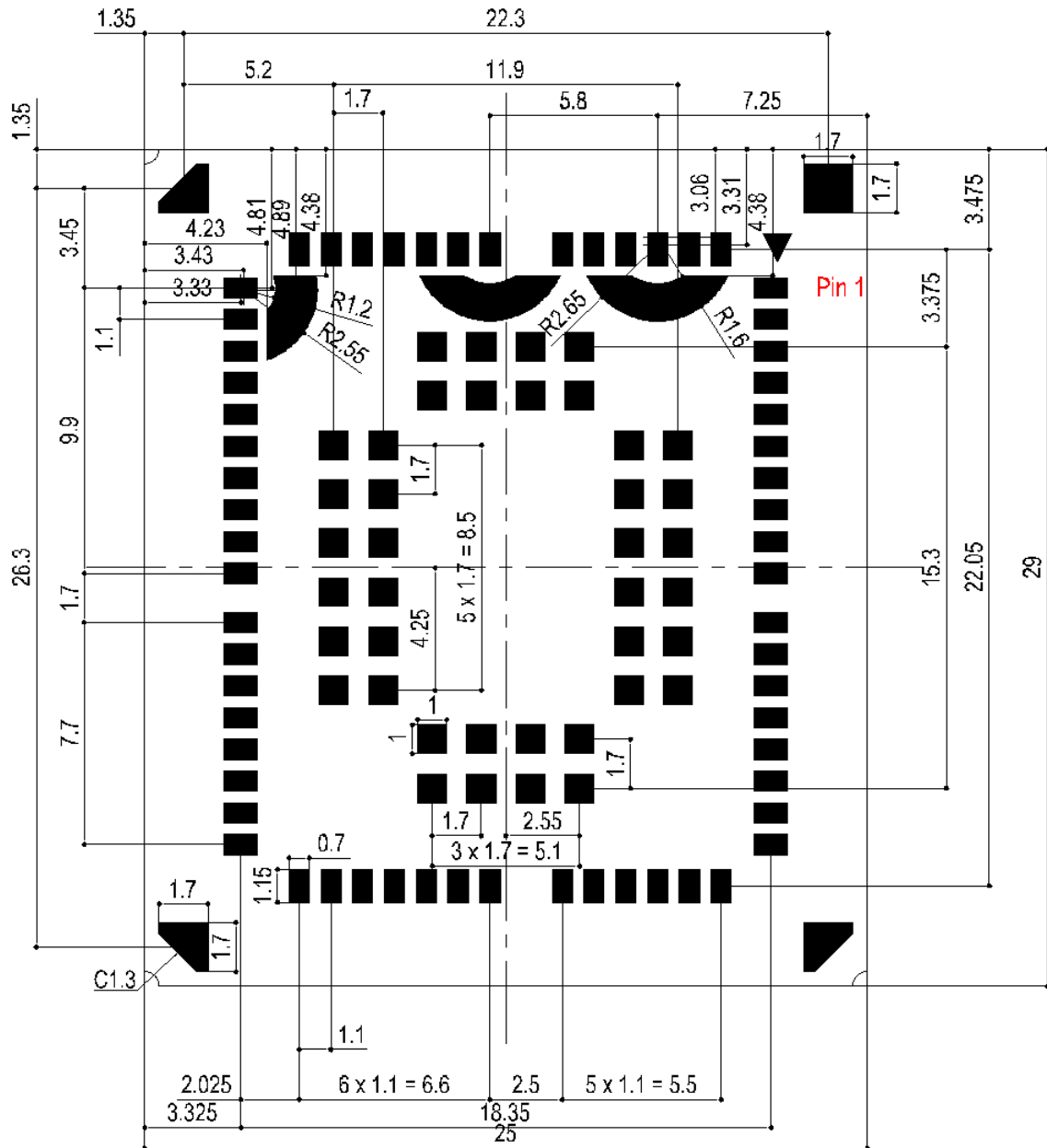


Figure 44: EG95-NA/-EX/-NAX/-NAXD/-AUX Bottom Dimensions (Top View)

**NOTE**

The package warpage level of the module conforms to *JEITA ED-7306* standard.

## 6.2. Recommended Footprint

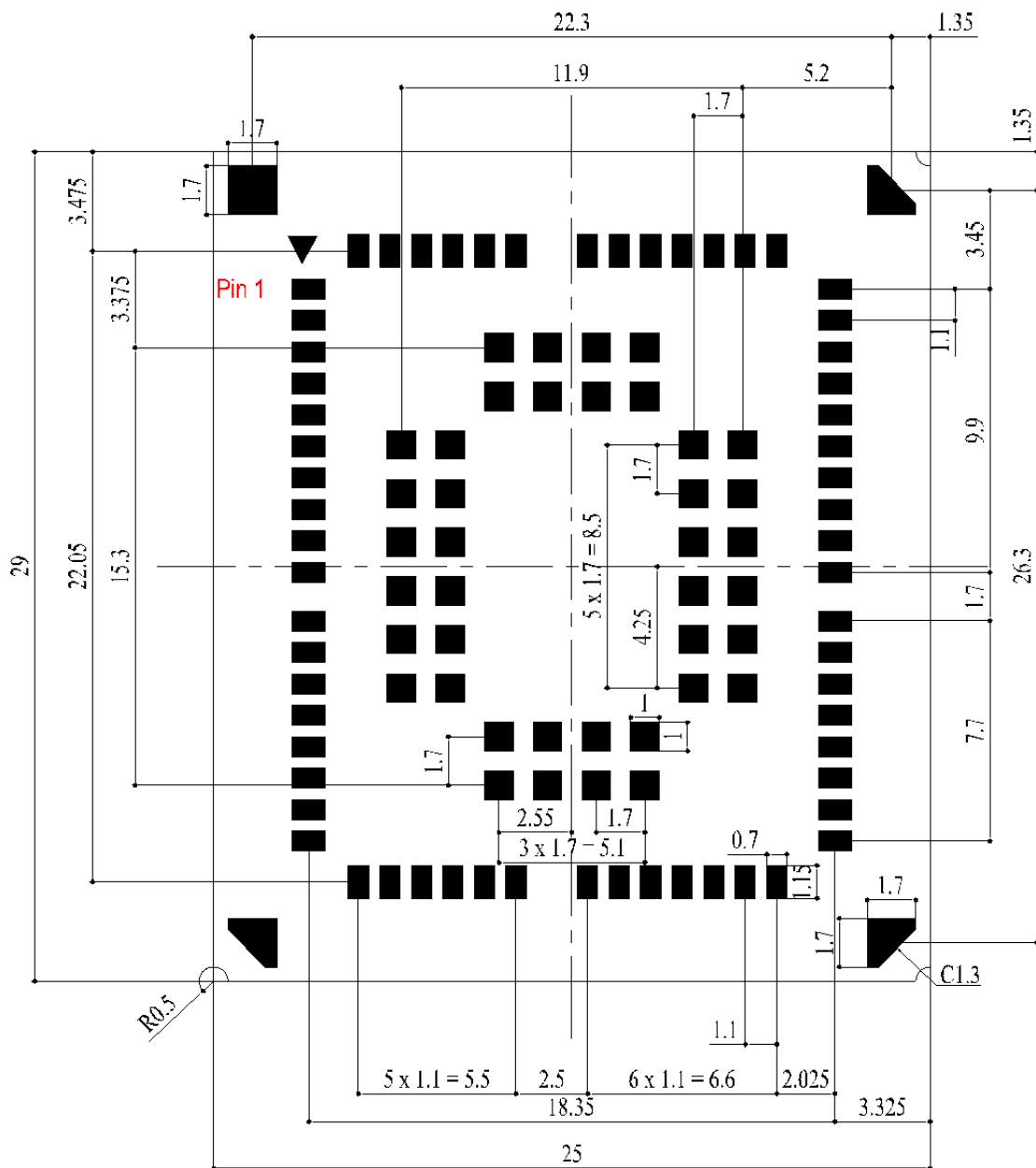
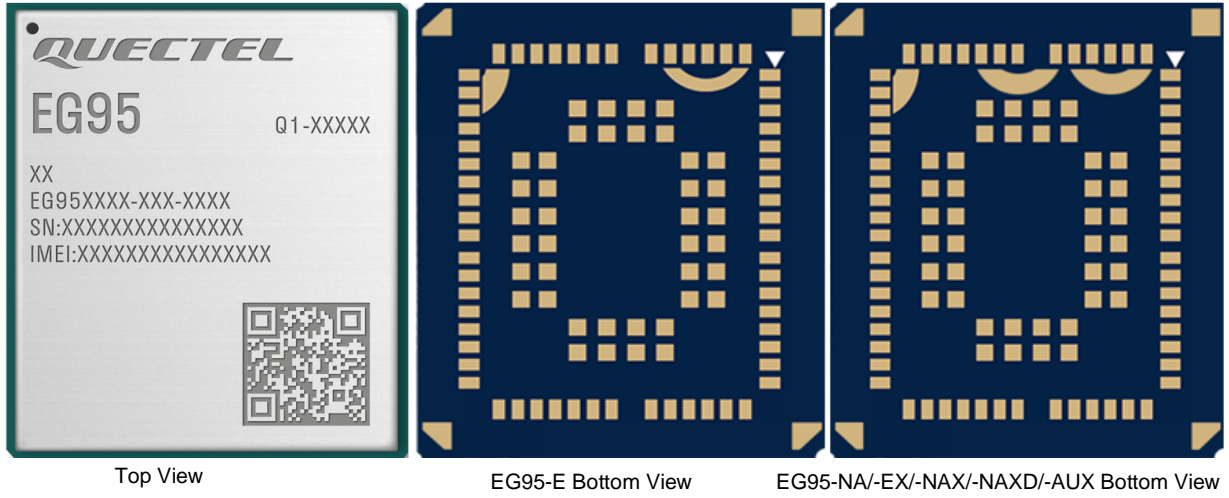


Figure 45: Recommended Footprint (Top View)

**NOTE**

For easy maintenance of this module, please keep about 3 mm between the module and other components on the motherboard.

### 6.3. Top and Bottom Views



**Figure 46: Top and Bottom Views of the Module**

**NOTE**

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Quectel.

# 7 Storage, Manufacturing and Packaging

## 7.1. Storage Conditions

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: the temperature should be  $23 \pm 5$  °C and the relative humidity should be 35–60 %.
2. Shelf life (in vacuum-sealed packaging): 12 months in Recommended Storage Condition.
3. Floor life: 168 hours <sup>12</sup> in a factory where the temperature is  $23 \pm 5$  °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g. a dry cabinet).
4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:
  - The module is not stored in Recommended Storage Condition;
  - Violation of the third requirement mentioned above;
  - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
  - Before module repairing.
5. If needed, the pre-baking should follow the requirements below:
  - The module should be baked for 8 hours at  $120 \pm 5$  °C;
  - The module must be soldered to PCB within 24 hours after the baking, otherwise it should be put in a dry environment such as in a dry cabinet.

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<sup>12</sup> This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. And do not remove the packages of tremendous modules if they are not ready for soldering.

**NOTE**

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

## 7.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. The force on the squeegee should be adjusted properly to produce a clean stencil surface on a single pass. To ensure the module soldering quality, the thickness of stencil for the module is recommended to be 0.13–0.15 mm. For more details, see **document [8]**.

The peak reflow temperature should be 235–246 °C, with 246 °C as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is strongly recommended that the module should be mounted only after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

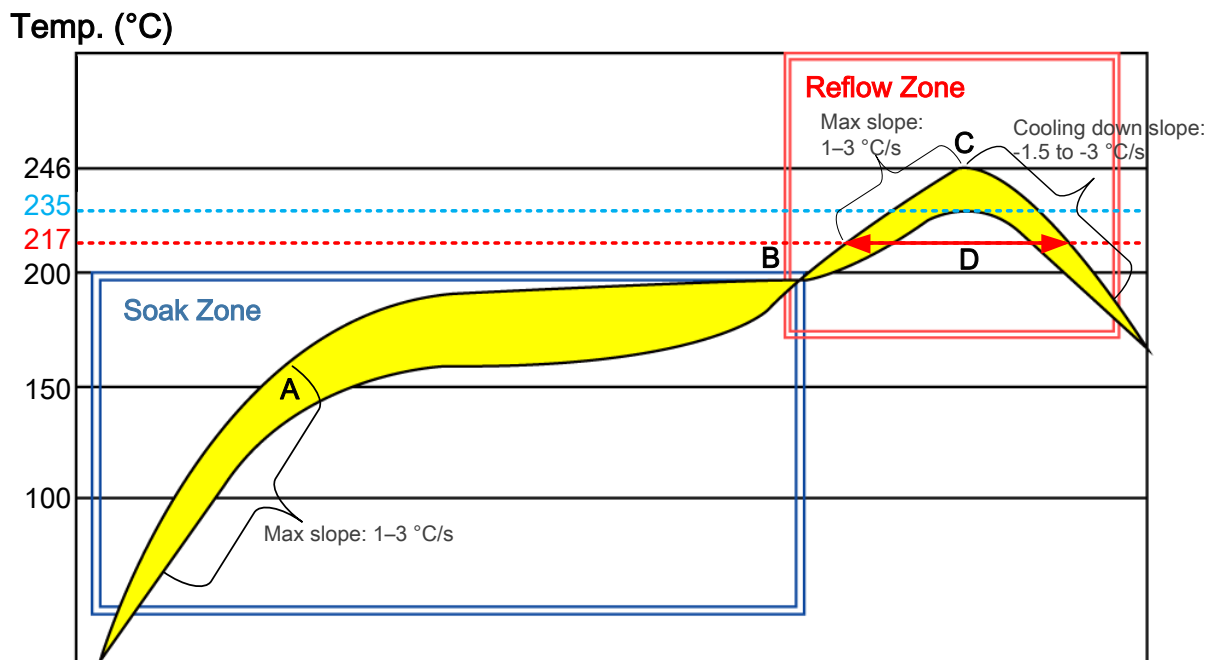


Figure 47: Recommended Reflow Soldering Thermal Profile

**Table 47: Recommended Thermal Profile Parameters**

Factor	Recommendation
<b>Soak Zone</b>	
Max slope	1–3 °C/s
Soak time (between A and B: 150 °C and 200 °C)	70–120 s
<b>Reflow Zone</b>	
Max slope	1–3 °C/s
Reflow time (D: over 217 °C)	40–70 s
Max temperature	235 °C to 246 °C
Cooling down slope	-1.5 to -3 °C/s
<b>Reflow Cycle</b>	
Max reflow cycle	1

**NOTE**

**1. EG95-E:**

- 1) During manufacturing and soldering, or any other processes that may contact the module directly, NEVER wipe the module’s shielding can with organic solvents, such as acetone, ethyl alcohol, isopropyl alcohol, trichloroethylene, etc. Otherwise, the shielding can may become rusted.
- 2) The shielding can for the module is made of Cupro-Nickel base material. It is tested that after 12 hours’ Neutral Salt Spray test, the laser engraved label information on the shielding can is still clearly identifiable and the QR code is still readable, although white rust may be found.

**2. EG95 Series (EG95-NA/-EX/-NAX/-NAXD/-AUX):**

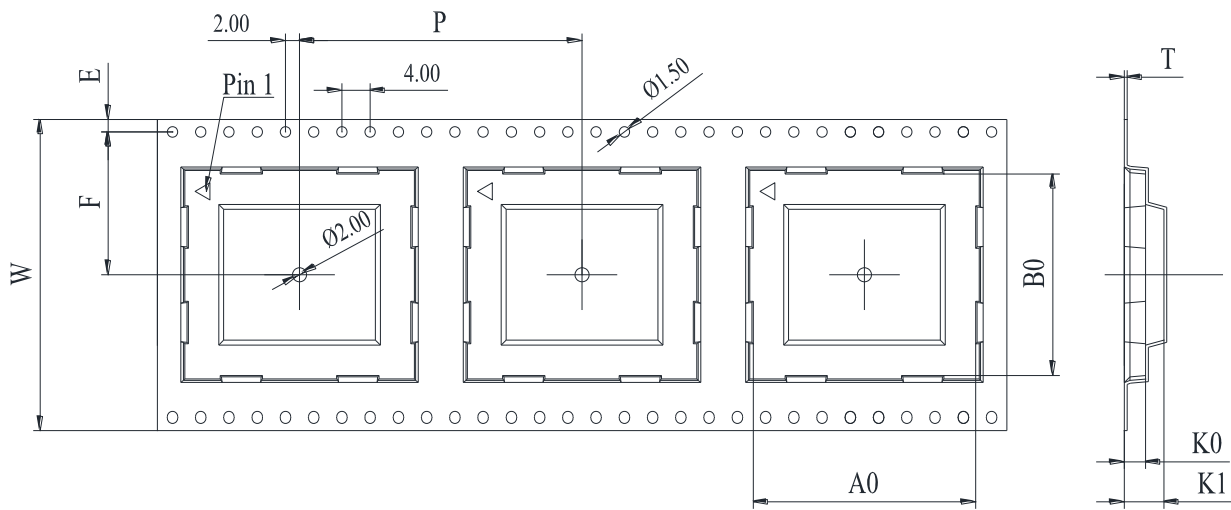
- 1) If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
- 2) Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
- 3) Due to the complexity of the SMT process, please contact Quectel Technical Supports in advance for any situation that you are not sure about, or any process (e.g. selective soldering, ultrasonic soldering) that is not mentioned in **document [8]**.

### 7.3. Packaging Specifications

The module adopts carrier tape packaging and details are as follow:

#### 7.3.1. Carrier Tape

Dimension details are as follow:



**Figure 48: Carrier Tape Dimension Drawing**

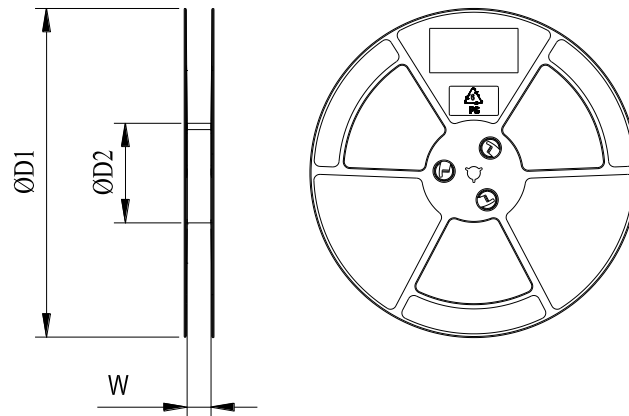
**Table 48: Carrier Tape Dimension Table (Unit: mm)**

W	P	T	A0	B0	K0	K1	F	E
44	32	0.35	25.5	29.5	3.2	5.8	20.2	1.75

**NOTE**

Actual pads in kind prevail when mounting.

**7.3.2. Plastic Reel**

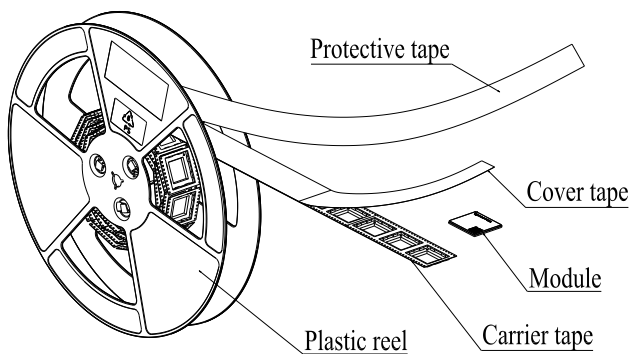


**Figure 49: Plastic Reel Dimension Drawing**

**Table 49: Carrier Tape Dimension Table (Unit: mm)**

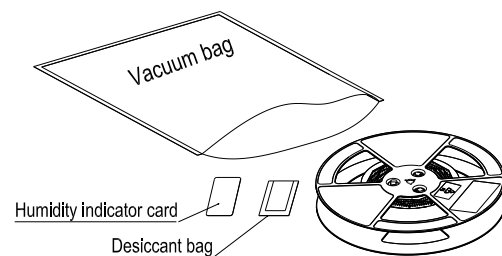
øD1	øD2	W
330	100	44.5

**7.3.3. Packaging Process**

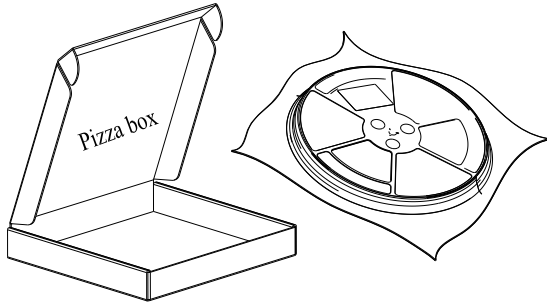


Place the module into the carrier tape and use the cover tape to cover them; then wind the heat-sealed carrier tape to the plastic reel and use the protective tape for protection. One plastic reel can load 250 modules.

Place the packaged plastic reel, humidity indicator card and desiccant bag into a vacuum bag, then vacuumize it.

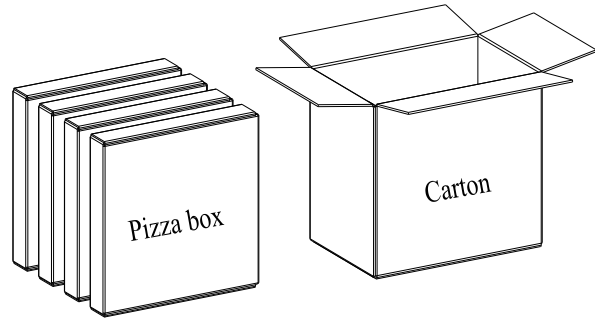






Place the vacuum-packed plastic reel into a pizza box.

Put 4 pizza boxes into 1 carton and seal it. One carton can pack 1000 modules.



**Figure 50: Packaging Process**

# 8 Appendix References

**Table 50: Related Documents**

Document Name
[1] Quectel_UMTS&LTE_EVB_User_Guide
[2] Quectel_EC2x&EG9x_Power_Management_Application_Note
[3] Quectel_EC2x&EG9x&EG2x-G&EM05_Series_AT_Commands_Manual
[4] Quectel_EC2x&EG9x&EG2x-G&EM05_Series_GNSS_Application_Note
[5] Quectel_EC2x&EG2x&EG9x&EM05_Series_QCFG_AT_Commands_Manual
[6] Quectel_RF_Layout_Application_Note
[7] Quectel_Module_Thermal_Design_Guide
[8] Quectel_Module_Secondary_SMT_Application_Note

**Table 51: Terms and Abbreviations**

Abbreviation	Description
ADC	Analog-to-Digital Converter
AMR	Adaptive Multi-rate
bps	Bits Per Second
CHAP	Challenge Handshake Authentication Protocol
CS	Coding Scheme
CSD	Circuit Switched Data
CTS	Clear To Send
DC-HSDPA	Dual-carrier High Speed Downlink Packet Access

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DC-HSPA+	Dual-carrier High Speed Packet Access
DCS	Data Coding Scheme
DFOTA	Delta Firmware Upgrade Over The Air
DL	Downlink
DTR	Data Terminal Ready
DTX	Discontinuous Transmission
EDGE	Enhanced Data Rates for GSM Evolution
EFR	Enhanced Full Rate
EGSM	Enhanced GSM
ESD	Electrostatic Discharge
FDD	Frequency Division Duplex
FR	Full Rate
FTP	File Transfer Protocol
FTPS	FTP over SSL
GLONASS	GLObalnaya NAVigatsionnaya Sputnikovaya Sistema, the Russian Global Navigation Satellite System
GMSK	Gaussian Minimum Shift Keying
GNSS	Global Navigation Satellite System
GPRS	General Packet Radio Service
GPS	Global Positioning System
GSM	Global System for Mobile Communications
HR	Half Rate
HSPA	High Speed Packet Access
HSDPA	High Speed Downlink Packet Access
HSUPA	High Speed Uplink Packet Access
HTTP	Hypertext Transfer Protocol

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HTTPS	Hypertext Transfer Protocol Secure
I/O	Input/Output
Inom	Nominal Current
LED	Light Emitting Diode
LGA	Land Grid Array
LNA	Low Noise Amplifier
LTE	Long Term Evolution
M2M	Machine to Machine
MCS	Modulation and Coding Scheme
ME	Mobile Equipment
MIMO	Multiple Input Multiple Output
MO	Mobile Originated
MMS	Multimedia Messaging Service
MS	Mobile Station (GSM engine)
MQTT	Message Queuing Telemetry Transport
MSL	Moisture Sensitivity Level
MT	Mobile Terminated
NITZ	Network Identity and Time Zone
NTP	Network Time Protocol
NMEA	NMEA (National Marine Electronics Association) 0183 Interface Standard
PA	Power Amplifier
PAM	Pulse-Amplitude Modulation
PAP	Password Authentication Protocol
PCB	Printed Circuit Board
PCM	Pulse Code Modulation

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PDA	Personal Digital Assistant
PDU	Protocol Data Unit
PING	Packet Internet Groper
PMIC	Power Management IC
POS	Point of Sale
PPP	Point-to-Point Protocol
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RHCP	Right Hand Circularly Polarized
RHCP	Right Hand Circularly Polarized
RoHS	Restriction of Hazardous Substances
Rx	Receive
SAW	Surface Acoustic Wave
SPI	Serial Peripheral Interface
SMD	Surface Mount Device
SMTP	Simple Mail Transfer Protocol
SMS	Short Message Service
SSL	Secure Sockets Layer
TCP	Transmission Control Protocol
TDD	Time Division Duplexing
TX	Transmitting Direction
UART	Universal Asynchronous Receiver/Transmitter.
UDP	User Datagram Protocol
UL	Uplink

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UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
(U)SIM	(Universal) Subscriber Identity Module
V <sub>max</sub>	Maximum Voltage
V <sub>nom</sub>	Nominal Voltage
V <sub>min</sub>	Minimum Voltage
V <sub>IHmax</sub>	Maximum High-level Input Voltage
V <sub>IHmin</sub>	Minimum High-level Input Voltage
V <sub>ILmax</sub>	Maximum Low-level Input Voltage
V <sub>ILmin</sub>	Minimum Low-level Input Voltage
V <sub>I,max</sub>	Absolute Maximum Input Voltage
V <sub>I,min</sub>	Absolute Minimum Input Voltage
V <sub>OHmin</sub>	Minimum High-level Output Voltage
V <sub>OLmax</sub>	Maximum Low-level Output Voltage
V <sub>OLmin</sub>	Minimum Low-level Output Voltage
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access

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