AG15 Reference Design

Automotive Module Series

Rev. AG15_Reference_Design_V1.2

Date: 2020-03-02

Status: Released

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About the Document

Revision History

Revision	Date	Author	Description
1.0	2019-01-10	Sea BAI/ Yeoman CHEN	Initial
1.1	2019-07-20	Jone CHEN	1. Updated the design diagram and notes in Sheet 1. 2. Changed the name of pin 91 from ANT_DIV to ANT_AUX. 3. Reserved pin 128. 4. Added a note about GPIO interfaces (Note 5 in Sheet 2). 5. Updated the reference design of PCIE_REFCLK signals (Sheet 2, Sheet 3). 6. Added a reference design for the connection between the module and the AP through USB (Sheet 3). 7. Updated the “DC-DC Application” diagram in Sheet 4. 8. Changed the recommended IMU sensor from SMI130 to IAM-20680, and thus also changed the IMU sensor design in Sheet 8. 9. Changed D0901 from LXES15AAA1-133 to LXES15AAA1-153 in Sheet 10.
1.2	2020-03-02	Jone CHEN	1. Changed the name of pin 96 from ANT_MAIN to ANT_CV2X_TRX0. 2. Changed the name of pin 91 from ANT_AUX to ANT_CV2X_TRX1. 3. Updated the notes in Sheet 10.

Contents

1 Reference Design

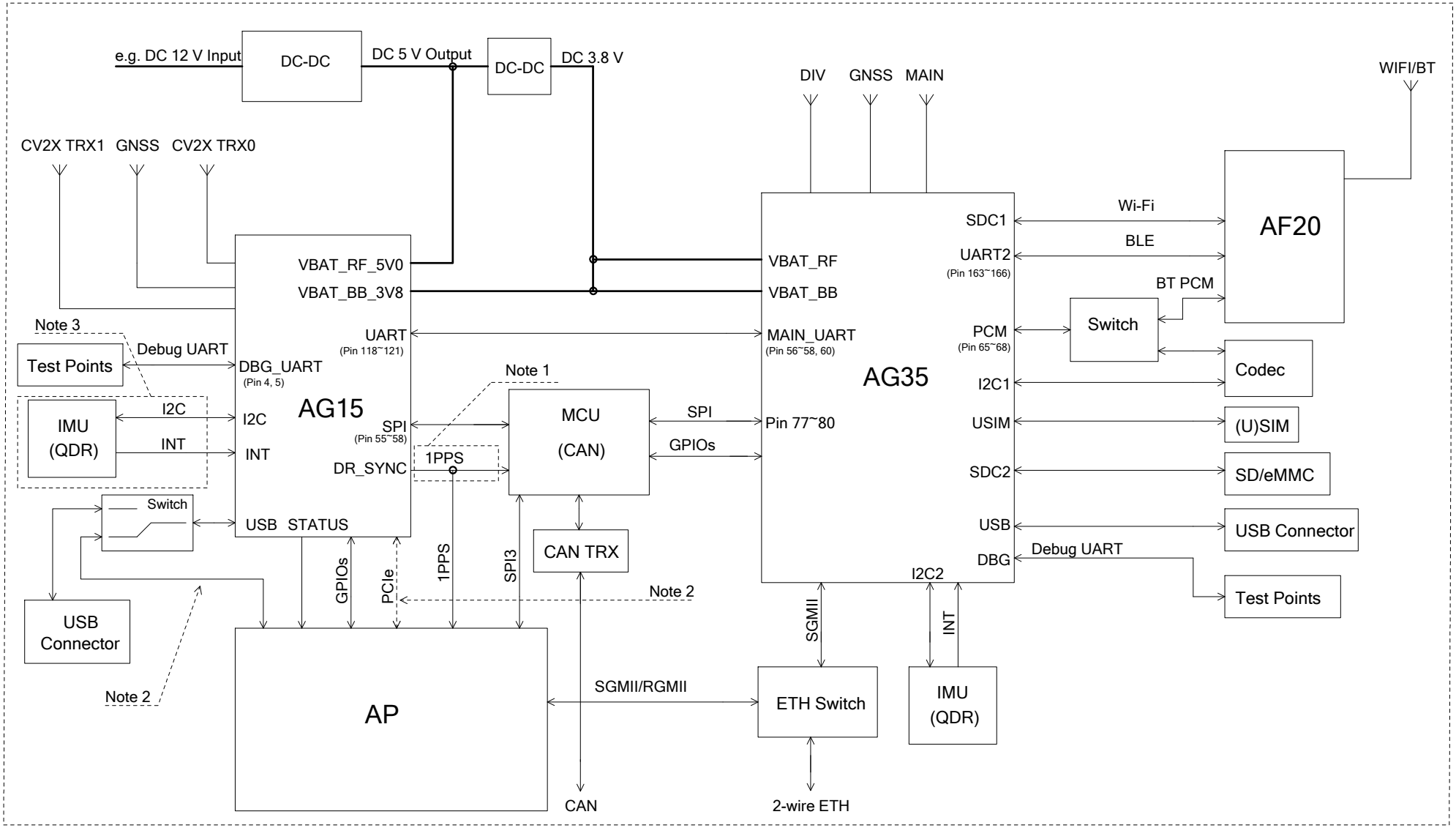
1.1. Introduction

This document provides reference designs of Quectel AG15 module.

1.2. Schematics

The schematics illustrated in the following pages are provided for your reference only.

Design Diagram for AG15+AG35



Notes:

1. A level translator should be added if the voltage level of customers' application is not 1.8 V.
2. USB is recommended for communication between AG15 and AP, and in such a case, PCIe is recommended to be reserved.
3. When AG15+AG35 solution is used, it is recommended to connect an IMU to AG35 and keep this IMU disconnected.

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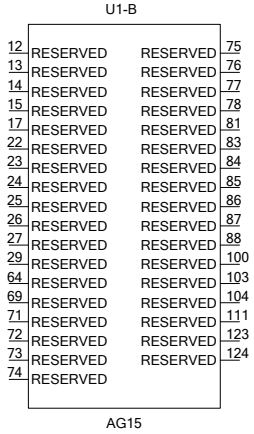
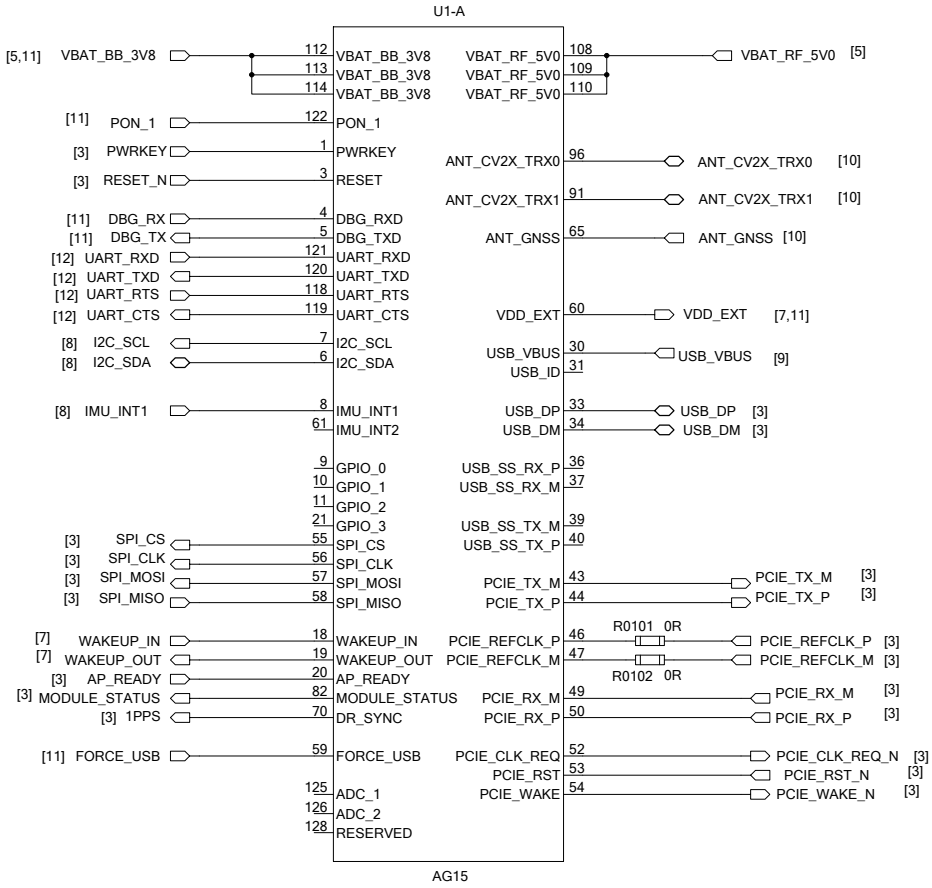
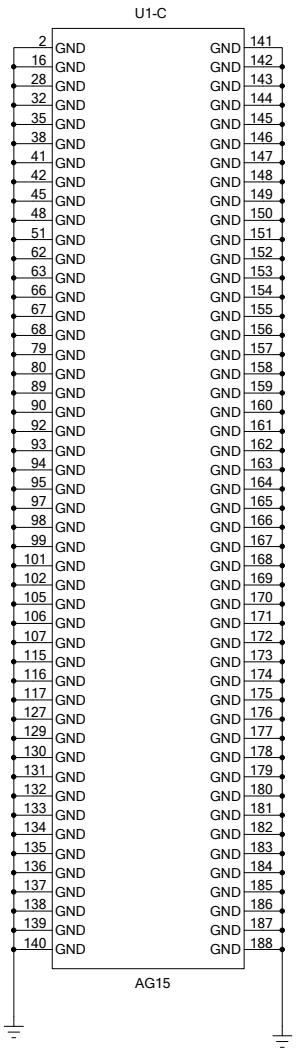
Module Interfaces







Notes:

1. ADC pins cannot be connected to the input power supply directly, and the input voltage of each ADC must not exceed its voltage range.
2. Keep all RESERVED and unused pins unconnected, and ensure all GND pins are connected to the ground network.
3. DR_SYNC is dead reckoning synchronization signal.
4. PCIe only supports endpoint mode.
5. GPIO_0 to GPIO_3 are designed for internal use only.

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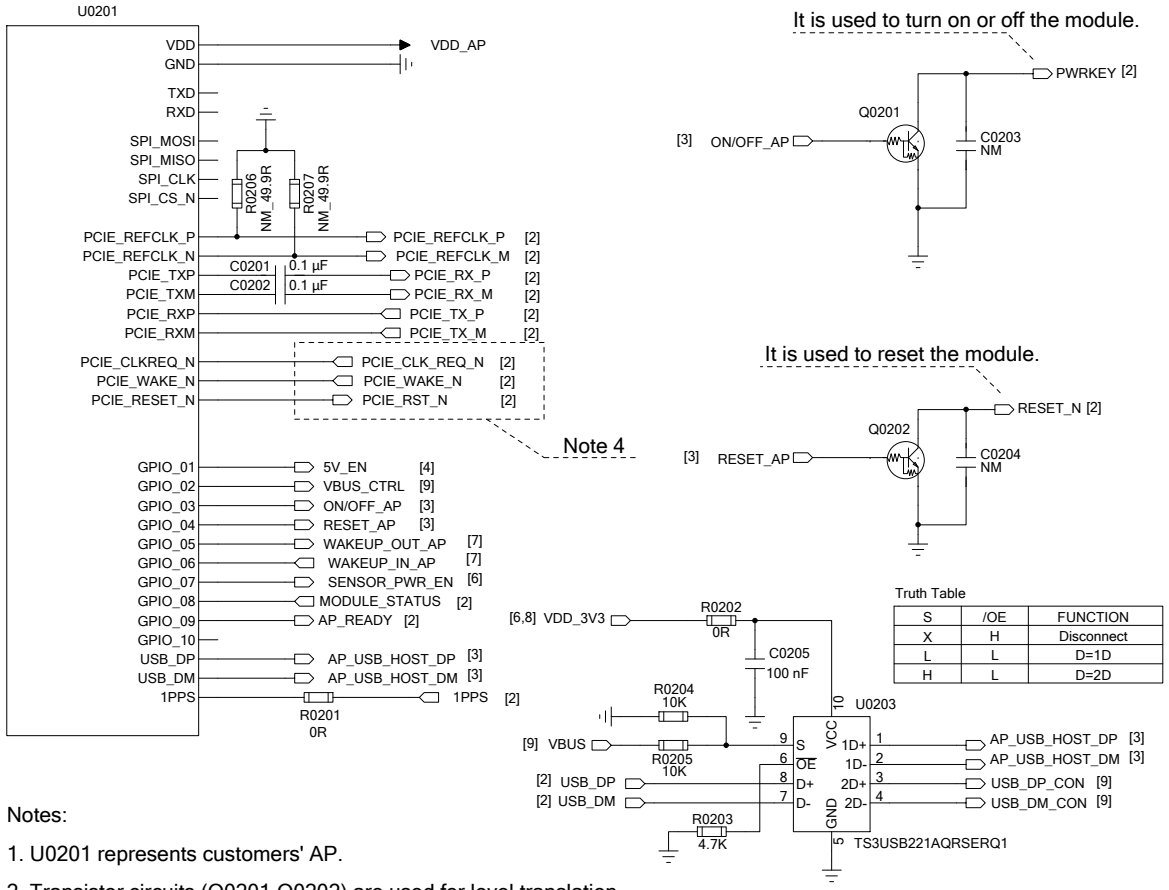
AP and SPI Interfaces

AP Interface



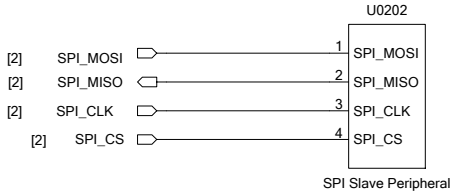
Truth Table

S	/OE	FUNCTION
X	H	Disconnect
L	L	D=1D
H	L	D=2D

Notes:

1. U0201 represents customers' AP.
2. Transistor circuits (Q0201-Q0202) are used for level translation.
3. WAKEUP_IN_AP should support wakeup function.
4. If the power domain of PCIe control signal is not 1.8 V, then a level translator should be designed.
5. If the power domain of 1PPS signal is not 1.8 V, then a level translator should be designed.
6. It is recommended to place R0206/R0207 close to the AP.

SPI Connection



Notes:

1. AG15 supports SPI master mode.
2. SPI interface of AG15 supports 1.8 V power domain only.

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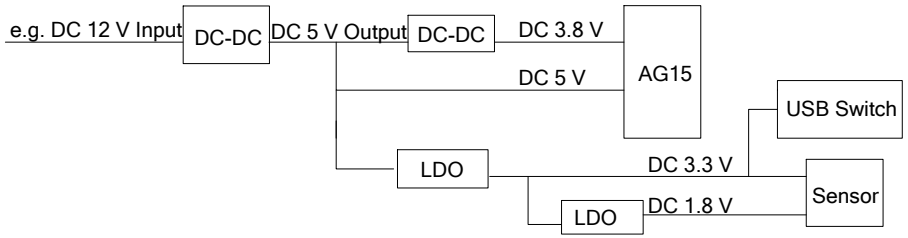
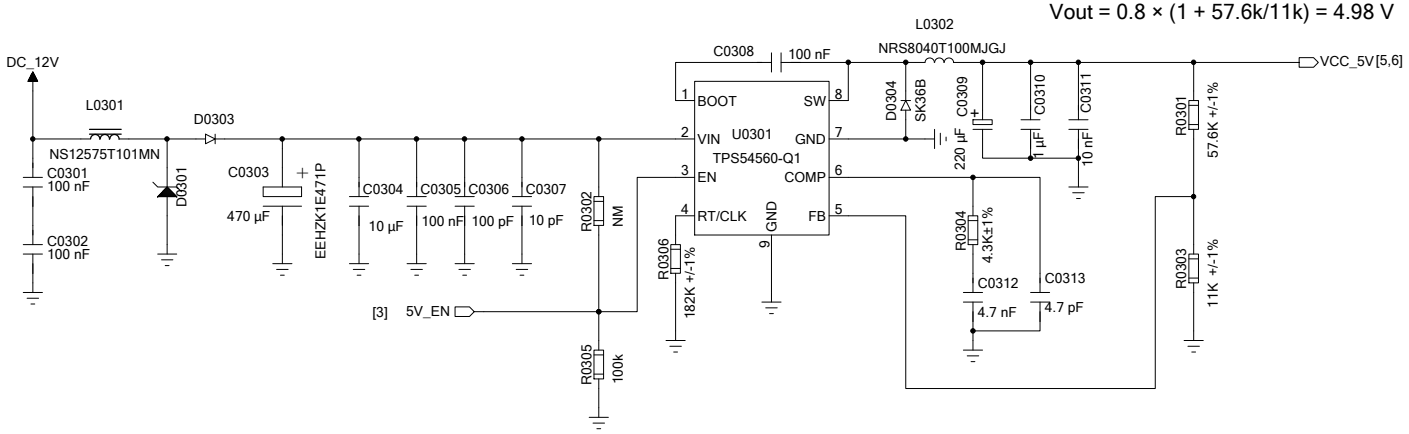
Power Supply Design (Part 1)

DC-DC Application

It is used when the input voltage is above 7 V. Use a DC-DC converter to convert a high input voltage to a 5 V output, and then generate 3.8 V, 3.3 V and 1.8 V typical voltages.



DC-DC Design



Note:

The power supply must be able to provide sufficient current up to 3 A or more.

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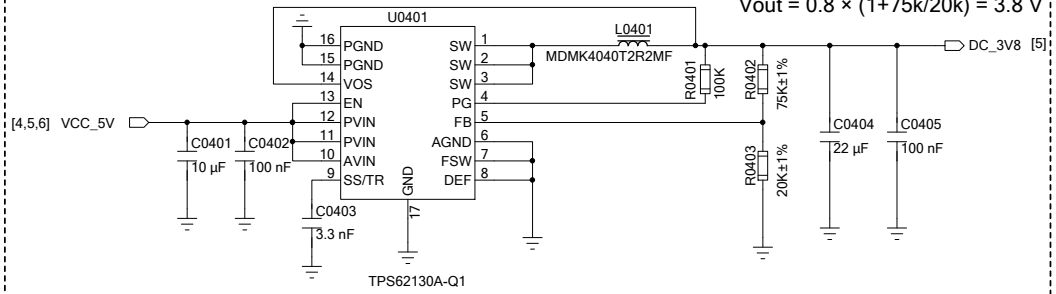
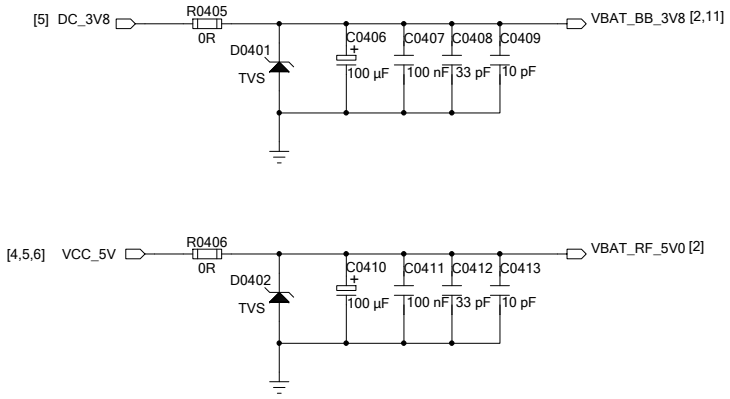
Power Supply Design (Part 2)

DC-DC Design



VBAT Design



Notes:

1. The recommended operating voltage of VBAT_BB_3V8 is 3.3 to 4.3 V.
2. The recommended operating voltage of VBAT_RF_5V0 is 4.75 to 5.25 V.
3. The TVS and decoupling capacitances should be placed close to the module's VBAT pins.

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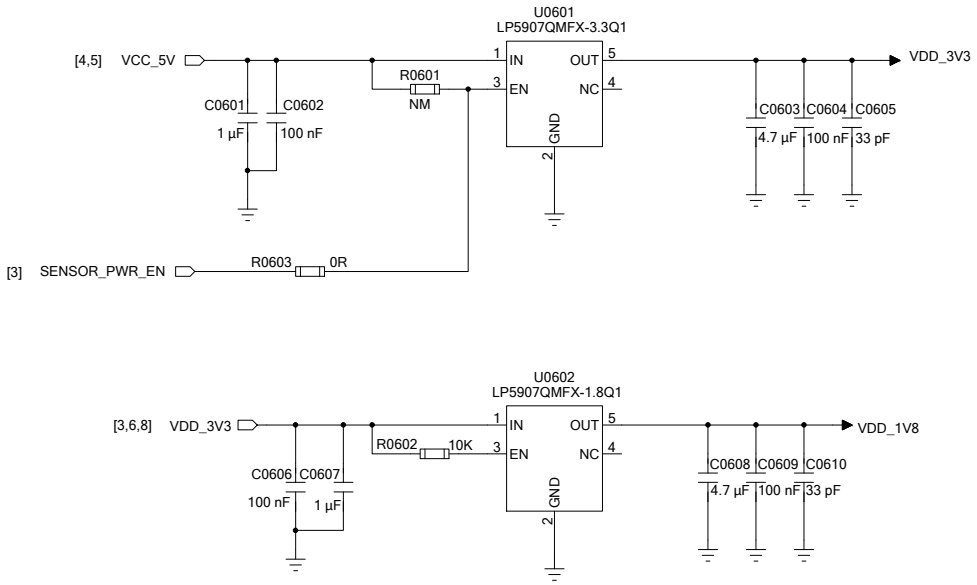
Power Supply Design (Part 3)

Supply Power for Sensor



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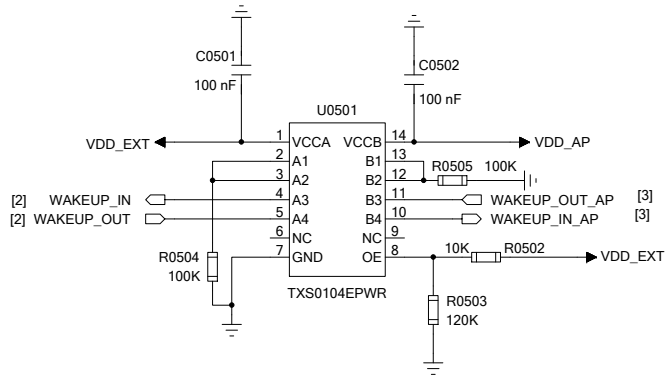
Level Translation Design

Translation - IC Solution



Notes:

1. A level translator circuit should be designed when the module interface provides a different power domain with customer applications.
2. The supply voltage range of VCCA should not exceed that of VCCB. For more information about TXS0104EPWR, please refer to the datasheet from TI.

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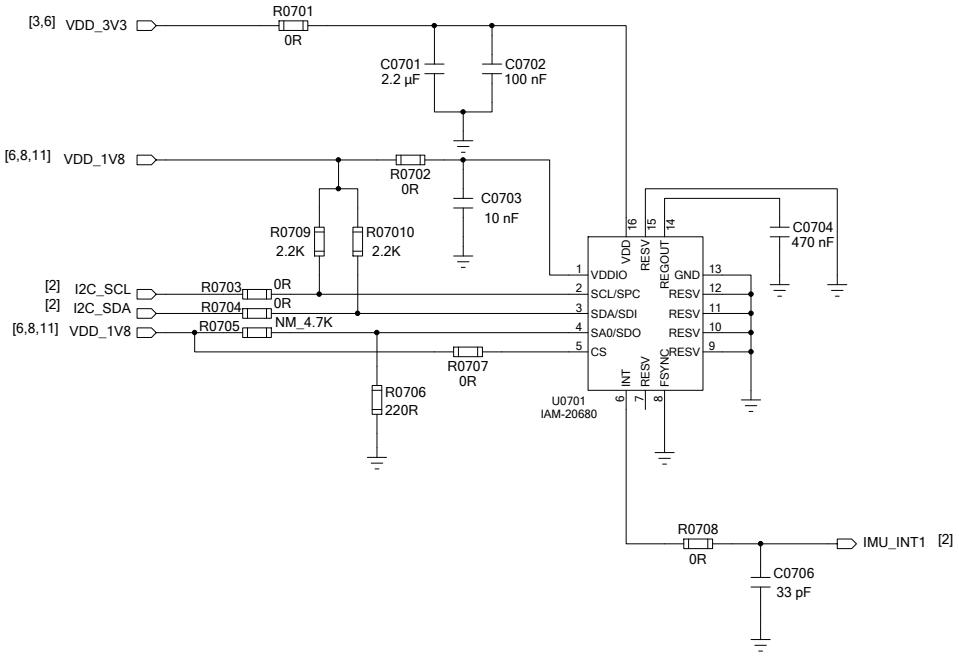
Sensor



IAM-20680 I2C Addresses		
SA0	0(Default)	1
I2C Addresses	0X68(1101000)	0X69(101001)

Note:

It is not recommended to place the sensor in direct vicinity of extremely hot spots regarding temperature as this can result in heating up the PCB and consequently also the sensor.

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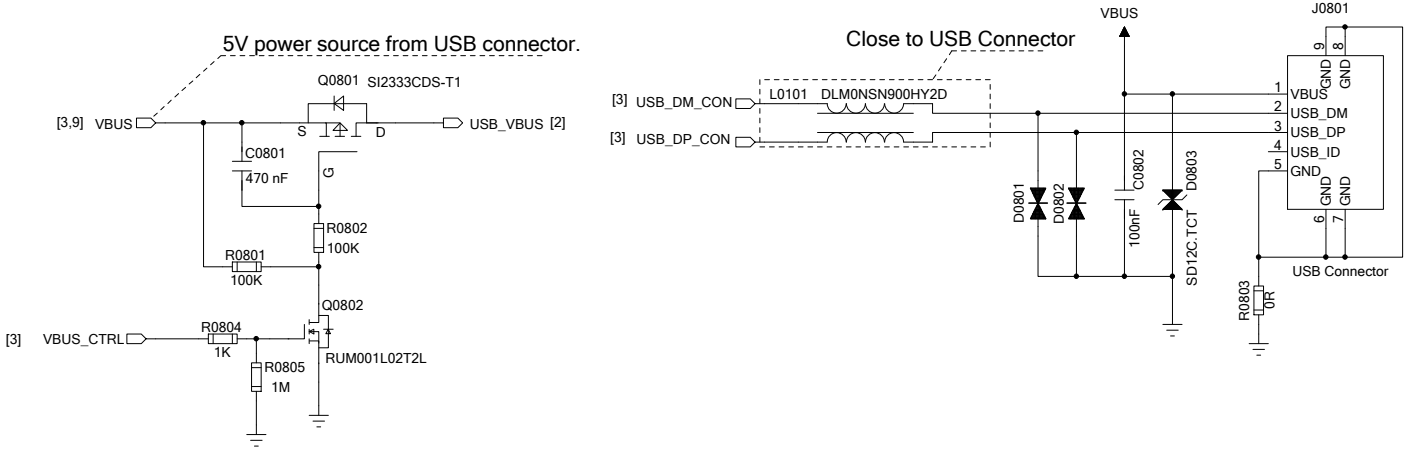
USB Interface



Notes:

1. AG15 supports USB 2.0 and USB 3.0.
2. The USB interface can be used to debug and upgrade firmware.
3. Please note that junction capacitance of ESD protection devices on USB data lines might influence the signal. Typically, the capacitance should be less than 1 pF.
4. USB_VBUS should be controllable. VBUS_CTRL is used to turn on/off USB_VBUS power supply. When VBUS_CTRL is at high level, USB_VBUS will be powered on.

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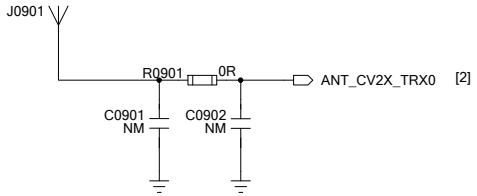
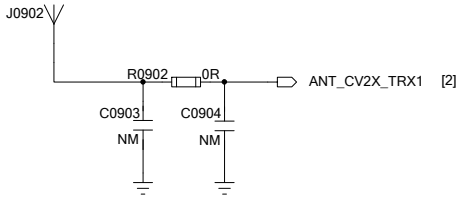
Antenna Designs

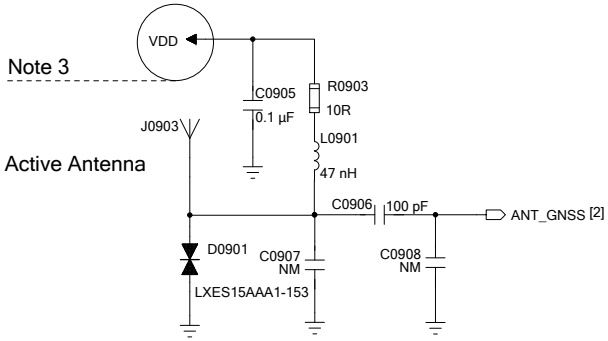
C-V2X TRX0 Antenna Interface



C-V2X TRX1 Antenna Interface



GNSS Antenna Interface



Notes:

1. The π type matching circuits are recommended to be reserved for C-V2X TRX0 and C-V2X TRX1 antenna circuits to facilitate future debugging.
2. When C-V2X works normally, TRX0 and TRX1 will switch automatically.
3. An external LDO can be used in active GNSS antenna circuit to supply power.
4. Passive GNSS antenna is not recommended in the design, as the antenna channel must use LNA to ensure normal operation of the module.
5. ESD protection devices should be added on the GNSS antenna interface, and the parasitic capacitance should be less than 0.05 pF.
6. Please control the impedance of the RF signal traces to 50 Ω while routing.

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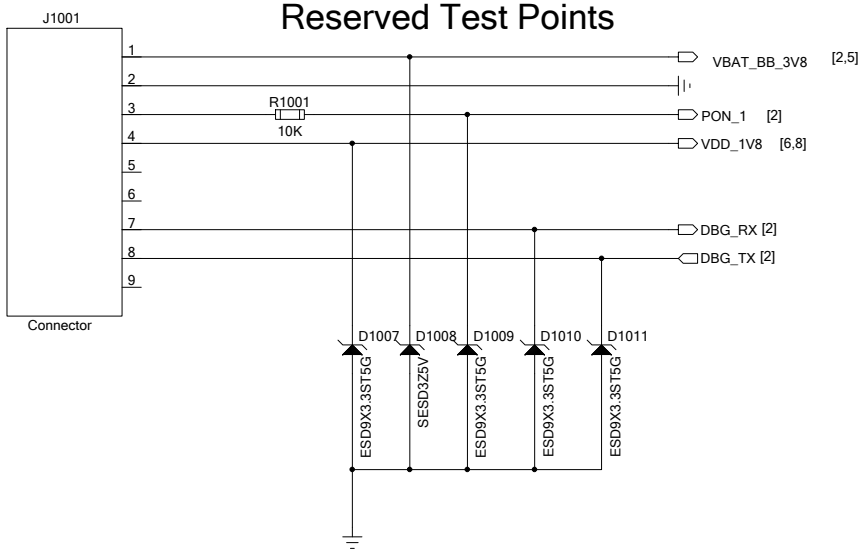
Test Points

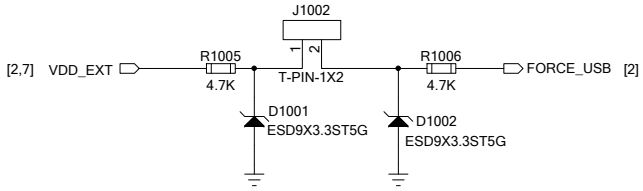
Reserved Test Points



Notes:

1. It is recommended to reserve test points for the debug UART interface so as to facilitate future software debugging.
2. The debug UART supports 1.8 V power domain.
   A level translator should be used if the power domain of customers' application is 3.3 V.
3. Pulling up PON_1 to 1.8V or VBAT_BB_3V8 will turn on the module.

Emergency Download Mode



Note:

Pulling up FORCE_USB to VDD_EXT before power-on will force the module into emergency download mode when power on.

Please keep it open when it is not used.

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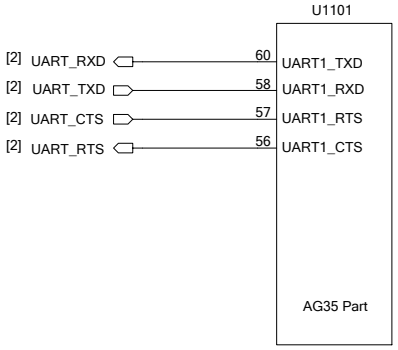
AG35 Connection



Note:

The above is only a sketch diagram illustrating the connection between AG15 and AG35. For more detailed designs of AG35, please refer to *Quectel_AG35_Reference Design/Quectel_AG35-QuecOpen_Reference Design*.

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