BG95 Reference Design

LPWA Module Series

Rev. BG95_Reference_Design_V1.0

Date: 2019-11-08

Status: Released

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GENERAL NOTES

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About the Document

History

Revision	Date	Author	Description
1.0	2019-11-08	Lyndon LIU/ Newgate HUA	Initial

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1 Reference Design

1.1. Introduction

This document provides reference designs of Quectel BG95 module, including power-on/off and reset scenarios, block diagrams, power supply, UART, (U)SIM and more interface designs.

1.2. Power-on/off and Reset Scenarios

1.2.1. Power-on Scenario

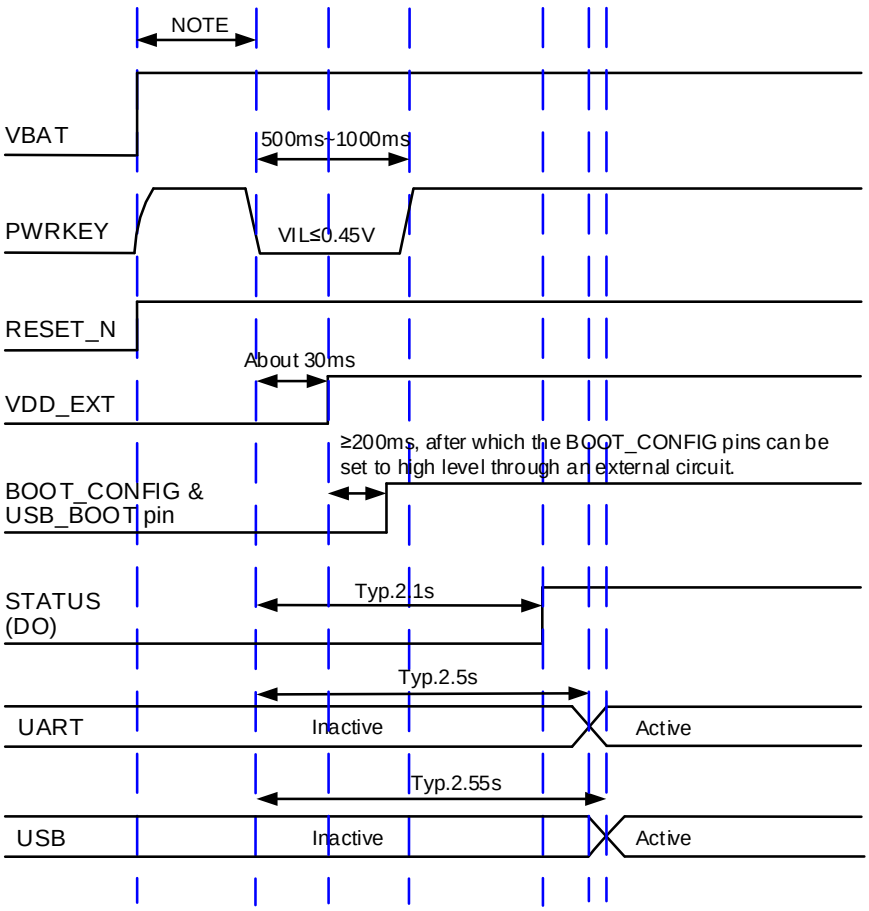


Figure 1: Timing of Turning on Module

NOTES

1. Make sure that VBAT is stable before pulling down PWRKEY pin and keep the interval no less than 30ms.
2. PWRKEY output voltage is 1.5V because of the voltage drop inside the Qualcomm chipset. Due to platform limitations, the chipset has integrated the reset function into PWRKEY. Therefore, PWRKEY should never be pulled down to GND permanently.

1.2.2. Power-off Scenario

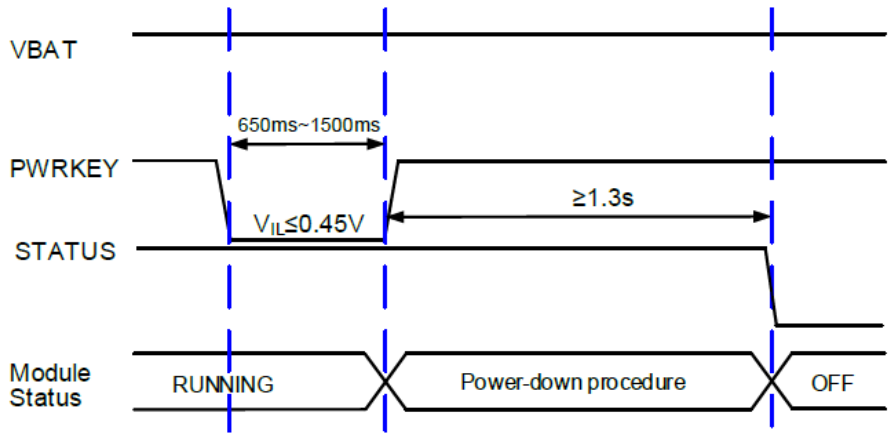


Figure 2: Timing of Turning off Module

1.2.3. Reset Scenario

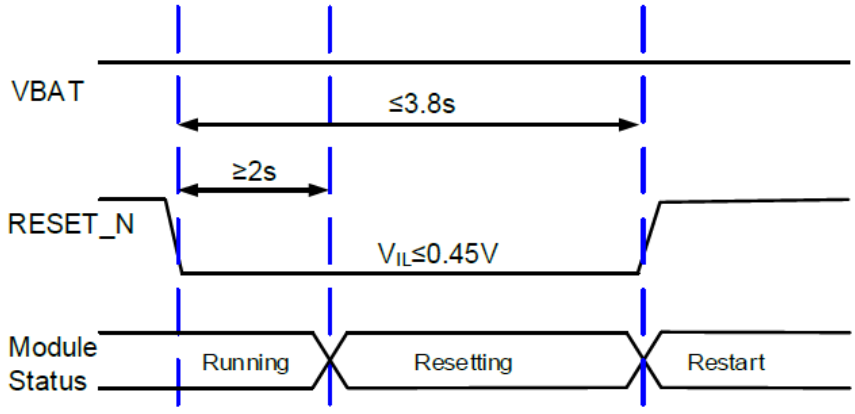


Figure 3: Timing of Resetting Module

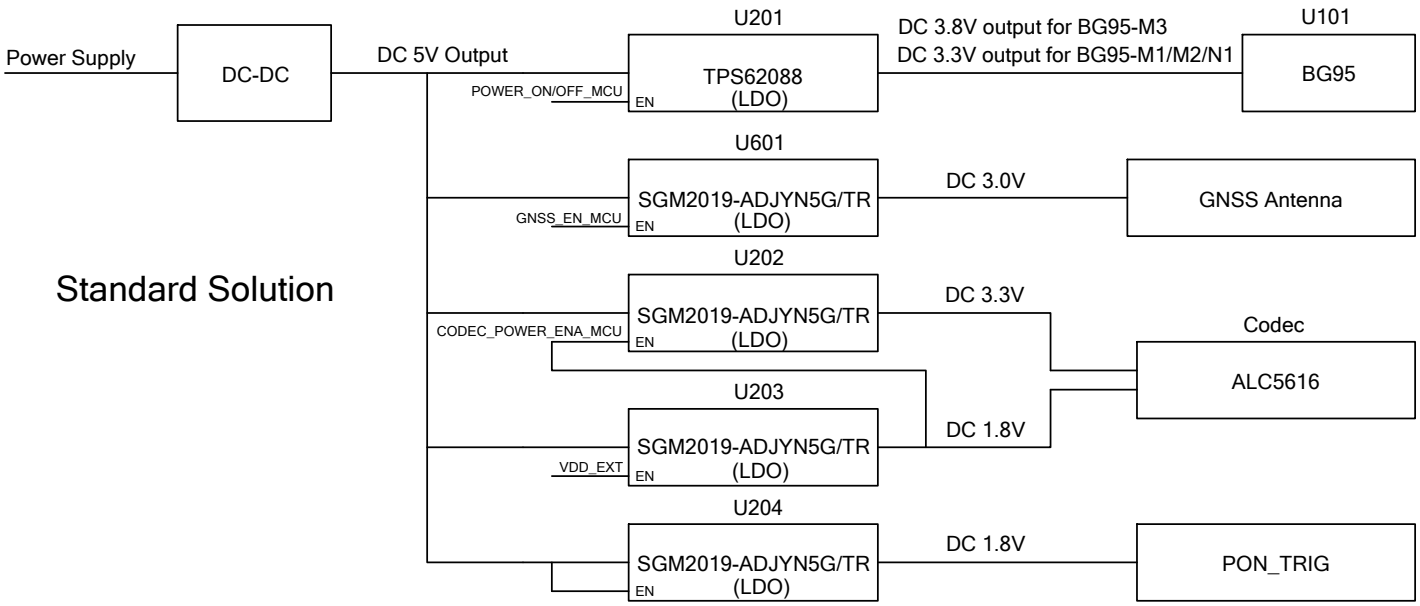
NOTE

Please assure that there is no large capacitance on RESET_N pin.

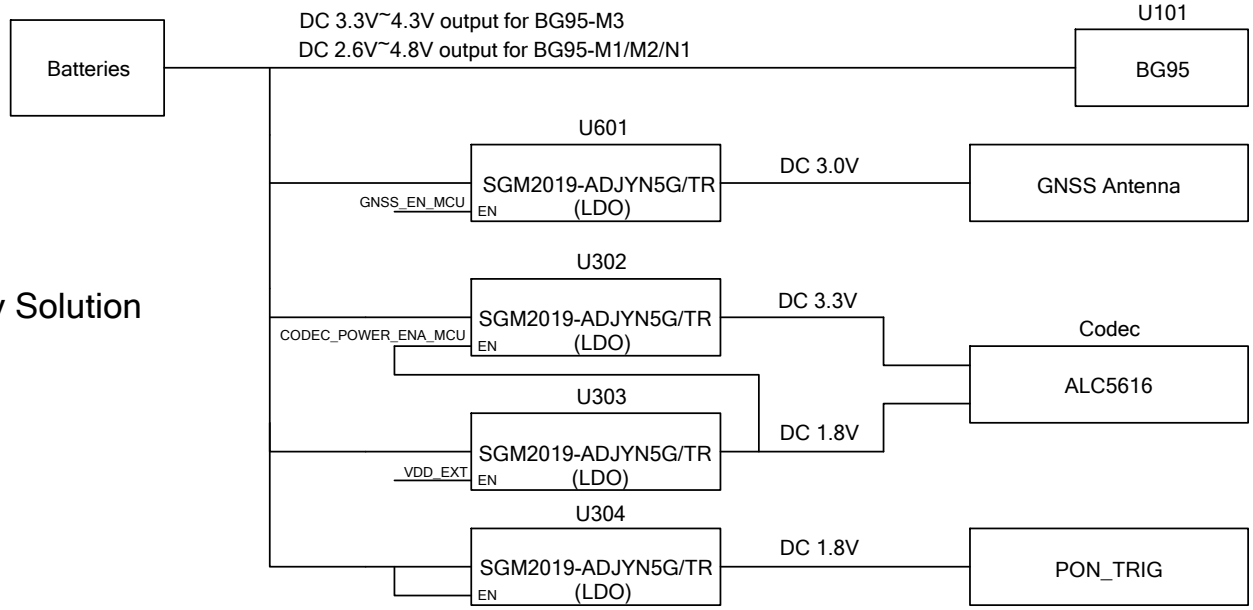
1.3. Schematics

The schematics illustrated in the following pages are provided for your reference only.

Power Supply Block Diagram



Standard Solution



Battery Solution

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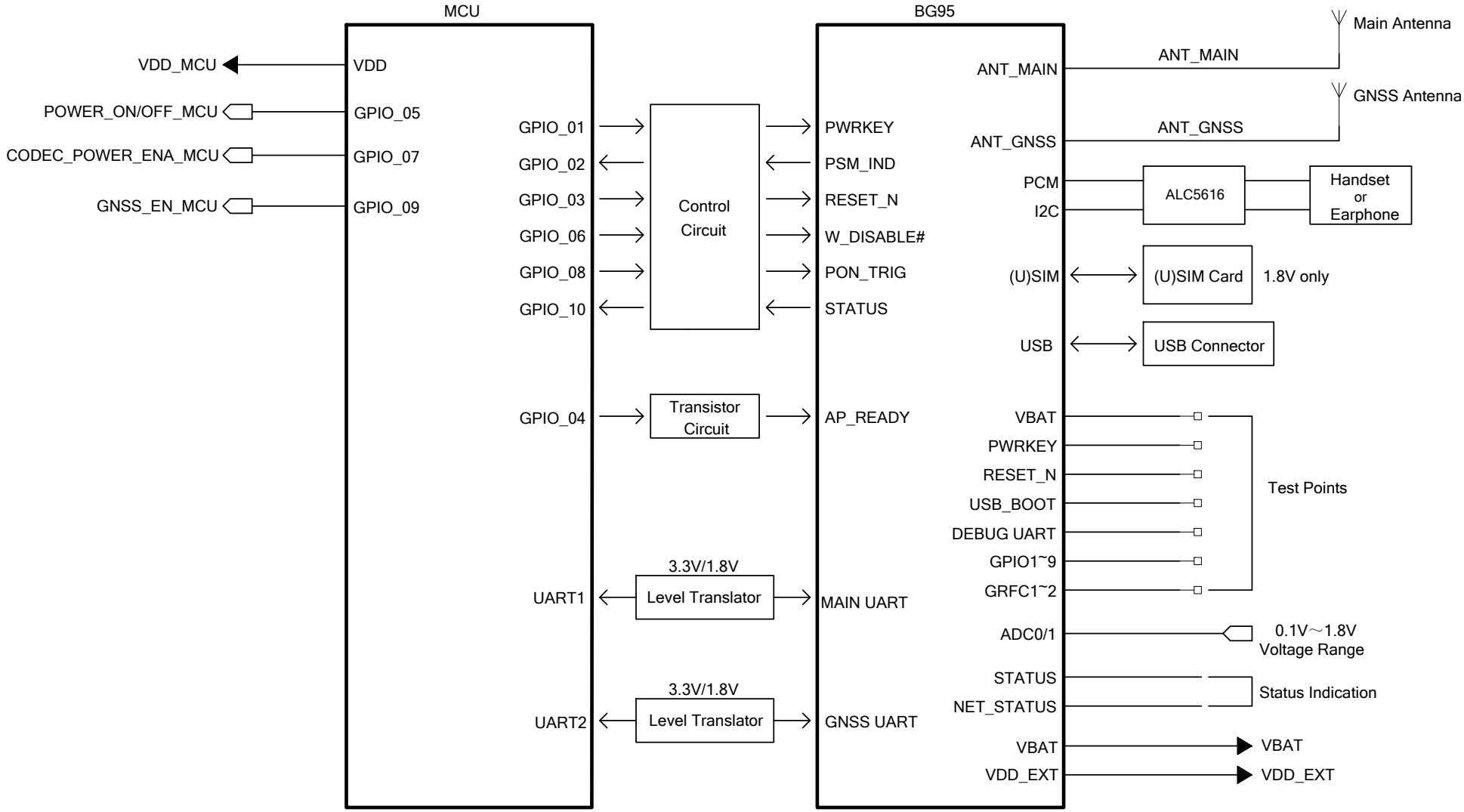
Reference Design Block Diagram



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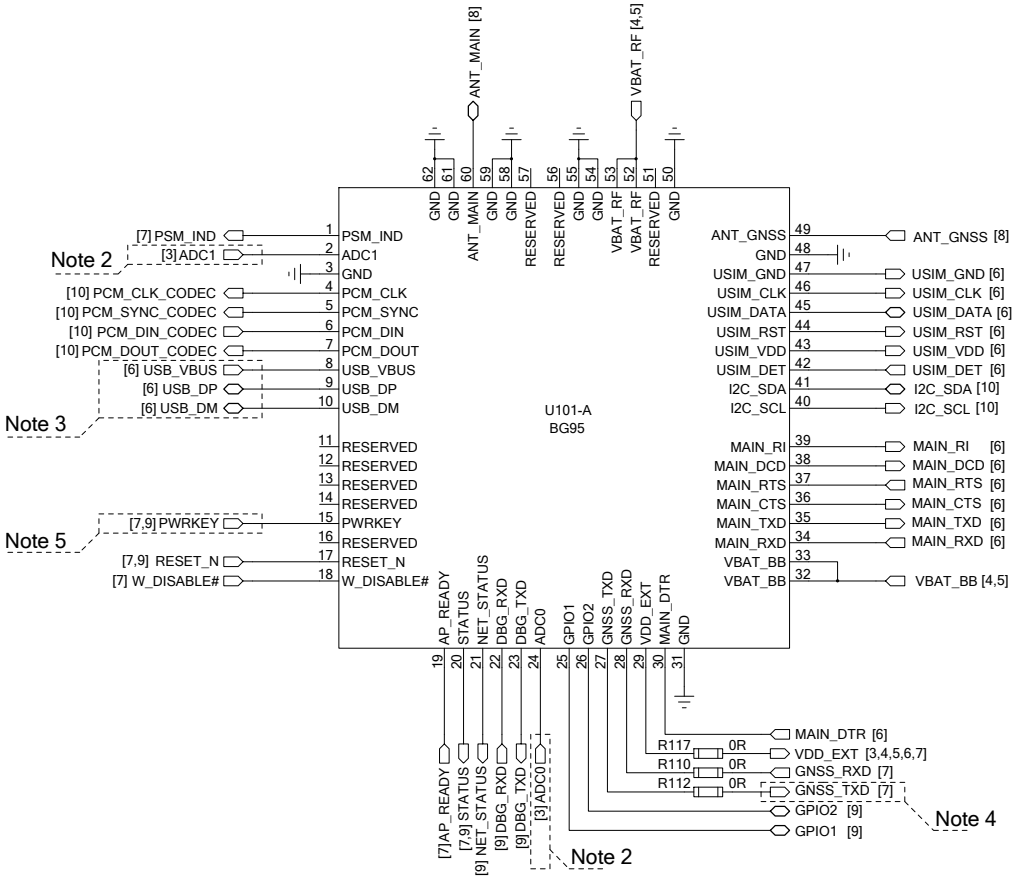
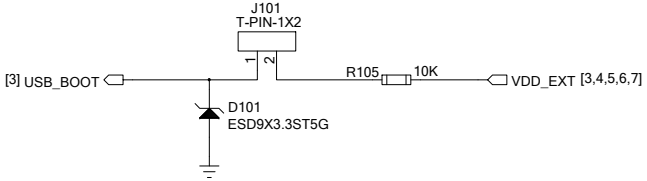
Module Interfaces

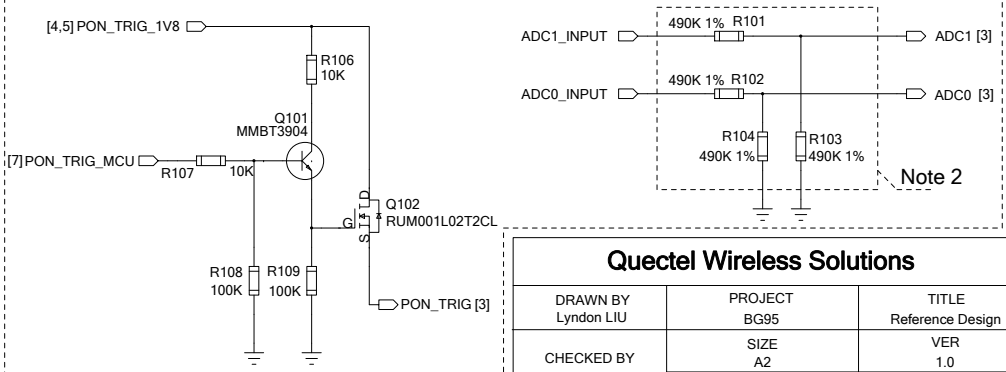


USB_BOOT Design



Note:
Pulling up USB_BOOT to VDD_EXT before startup, the module will be forced into emergency download mode when it is powered on.

PON_TRIG and ADC Designs



Notes:

1. Keep all RESERVED and unused pins unconnected, and all GND pins should be connected to ground.
2. ADC pin cannot be directly connected to the power supply and must not exceed 1.8V.
   ADC0 and ADC1 cannot be used simultaneously. BG95 supports using of only one ADC interface at a time: either ADC0 or ADC1. It is recommended to use resistor divider circuit for ADC application, and the divider resistor accuracy should be no less than 1%.
3. BG95 can only work as a USB device and supports Low Speed and Full Speed modes.
   The USB interface is primarily used for AT command communication, software debugging and firmware upgrade. The input voltage range of USB_VBUS is 3.0V~5.25V.
4. GNSS_TXD and GRFC2 are BOOT_CONFIG pins. They should not be pulled up before startup.
5. PWRKEY should never be pulled down to GND permanently.
6. When PON_TRIG detects a rising edge, the module will be woken up from PSM (Power Saving Mode). PON_TRIG is pulled down by default.

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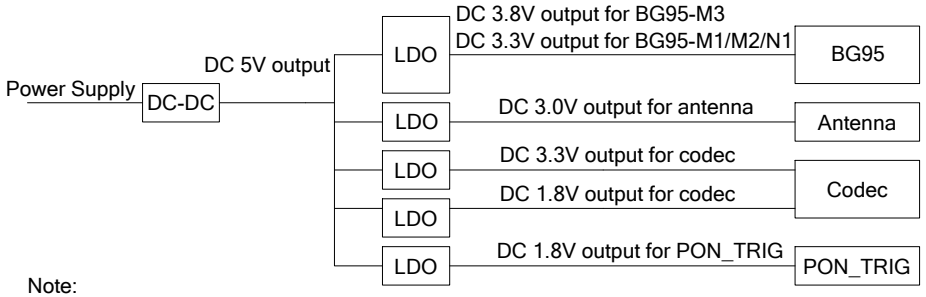
Power Supply Design (Standard Solution)

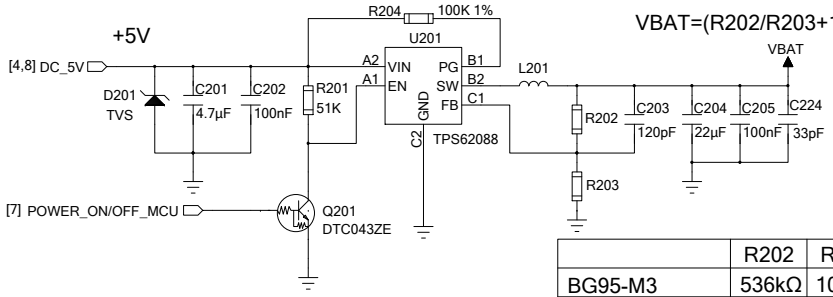
DC-DC Application

This solution is used when the input voltage is above 7V. First use a DC-DC converter to convert the high input voltage into a 5V output, and then the LDO will generate a 3.3V typical voltage for BG95-M1/M2/N1 and 3.8V typical voltage for BG95-M3.



Note:
Customers can select either standard power supply design or battery power supply solution according to their specific application demands.

LDO Design

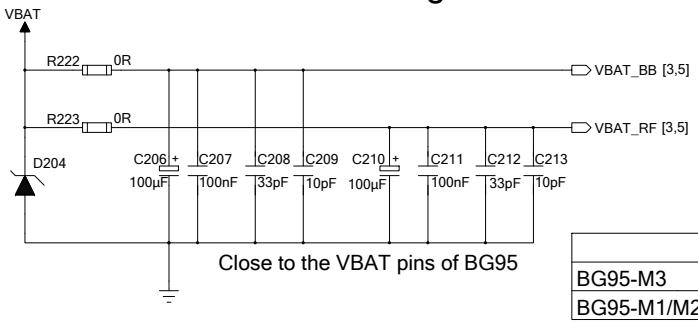


	R202	R203	L201
BG95-M3	536kΩ	100kΩ	330nH
BG95-M1/M2/N1	453kΩ	100kΩ	360nH

Precision of resistance +/-1%

Note:
This solution is used when the input voltage is below 5.5V.

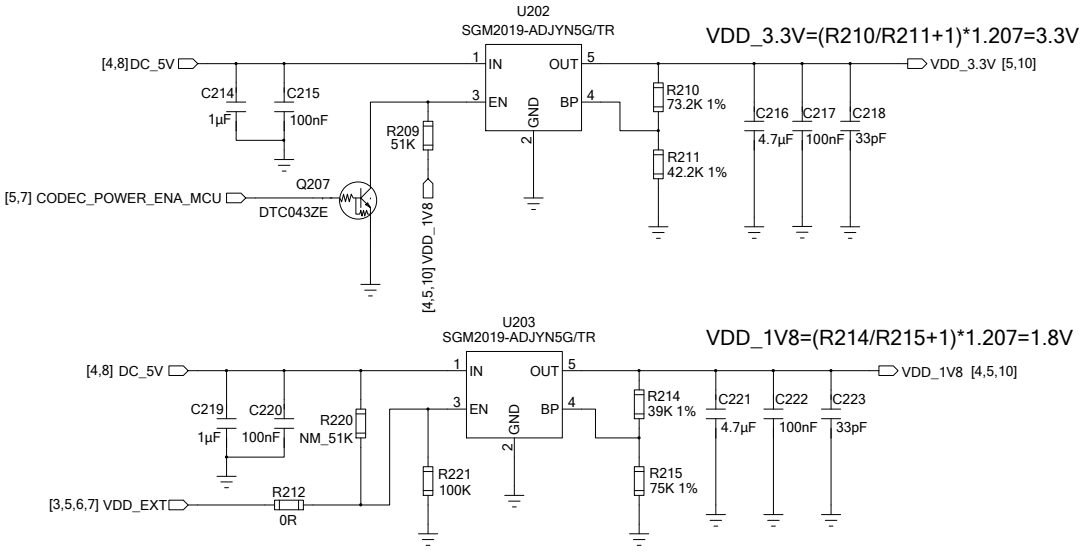
VBAT Design



	D204
BG95-M3	WS4.5DPV
BG95-M1/M2/N1	WS05DP

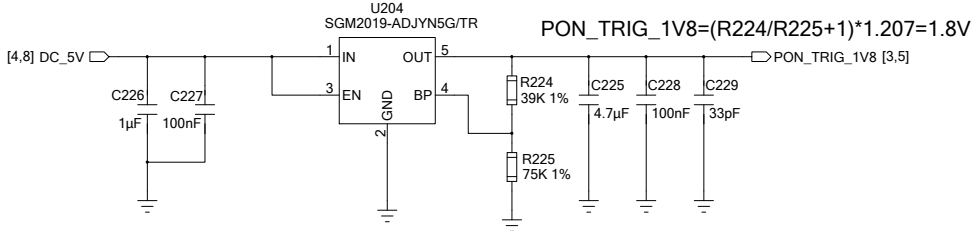
Note:
VBAT should be routed in star structure to VBAT_BB and VBAT_RF pins.

Power Supply for Audio Codec



Notes:
1. CODEC_POWER_ENA_MCU must be at low level in order to ensure the normal output voltage of VDD_3.3V. If VDD_3.3V power supply needs to be switched off, please keep CODEC_POWER_ENA_MCU at high level.
2. To ensure that the audio codec works normally, please follow the power-on and power-off sequences of its power supply.
   Power ON Sequence: power on VDD_1V8 first, and then VDD_3V3.
   Power OFF Sequence: power off VDD_3V3 first, and then VDD_1V8.

Power Supply for PON_TRIG



Note:
PON_TRIG is powered by an external LDO.

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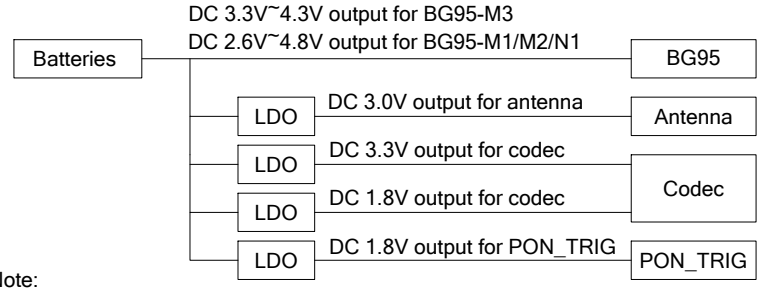
Power Supply Design (Battery Solution)

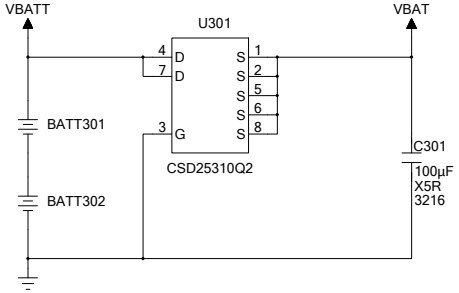
Battery Application

The following is the block diagram for battery application.
The output voltage of batteries must be kept between 2.6V and 4.8V (BG95-M1/M2/N1).
The output voltage of batteries must be kept between 3.3V and 4.3V (BG95-M3).

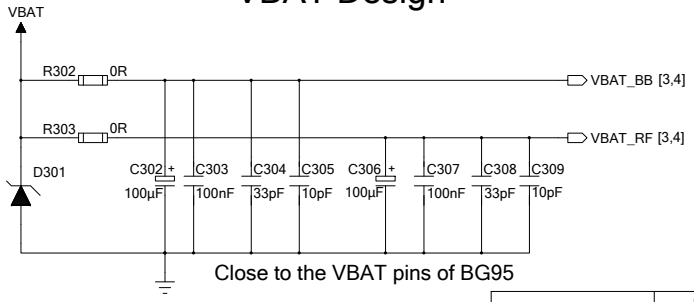


Note:
Customers can select either standard power supply design or battery power supply solution according to their specific application demands.

Battery Polarity Protection for BG95



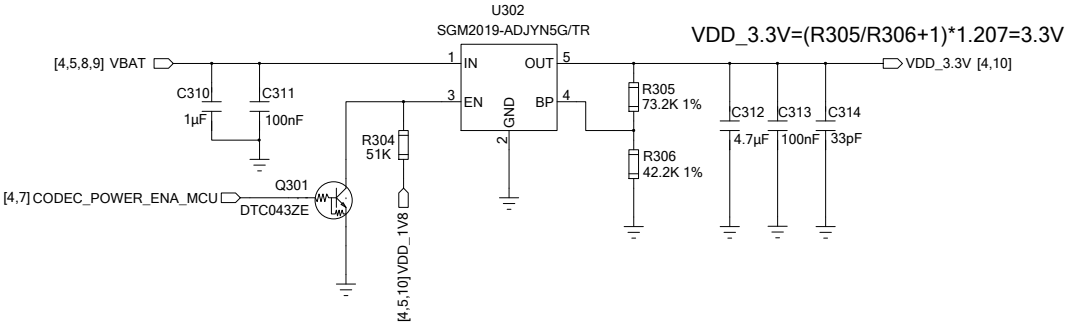
VBAT Design

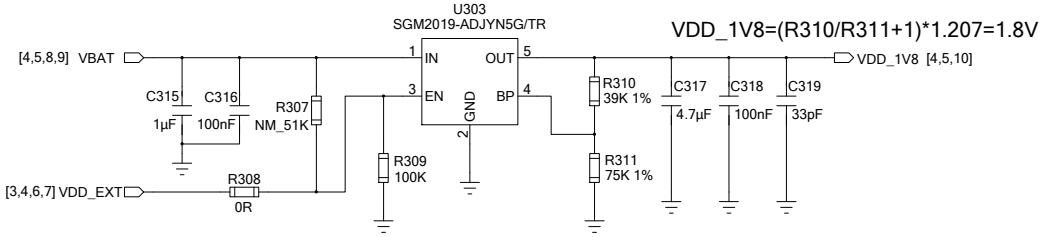


	D301
BG95-M3	WS4.5DPV
BG95-M1/M2/N1	WS05DP

Note:
VBAT should be routed in star structure to VBAT_BB and VBAT_RF pins.

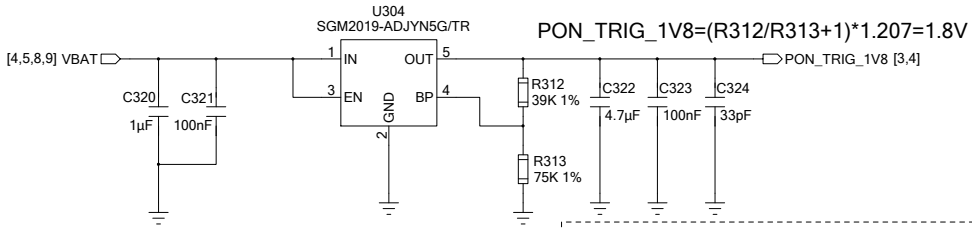
Power Supply for Audio Codec





Notes:
1. CODEC_POWER_ENA_MCU must be at low level in order to ensure the normal output voltage of VDD_3.3V.
   If VDD_3.3V power supply needs to be switched off, please keep CODEC_POWER_ENA_MCU at high level.
2. To ensure that the audio codec works normally, please follow the power-on and power-off sequences of its power supply.
   Power ON Sequence: power on VDD_1V8 first, and then VDD_3V3.
   Power OFF Sequence: power off VDD_3V3 first, and then VDD_1V8.

Power Supply for PON_TRIG



Note:
PON_TRIG is powered by an external LDO.

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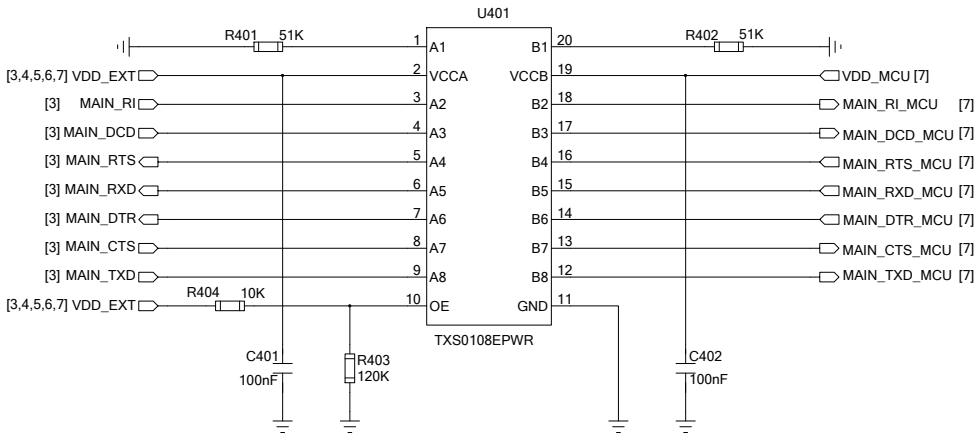
UART, USB and (U)SIM Designs

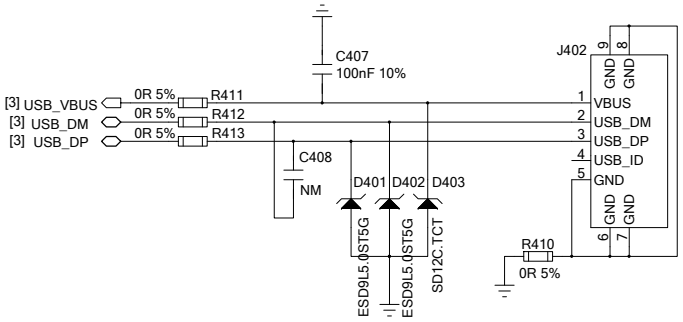
UART Level Translator



Notes:

1. TXS0108EPWR is used to realize the voltage level translation between BG95 and MCU.
2. VCCA should not exceed VCCB. For more information about TXS0108EPWR, please refer to the datasheet from TI website.

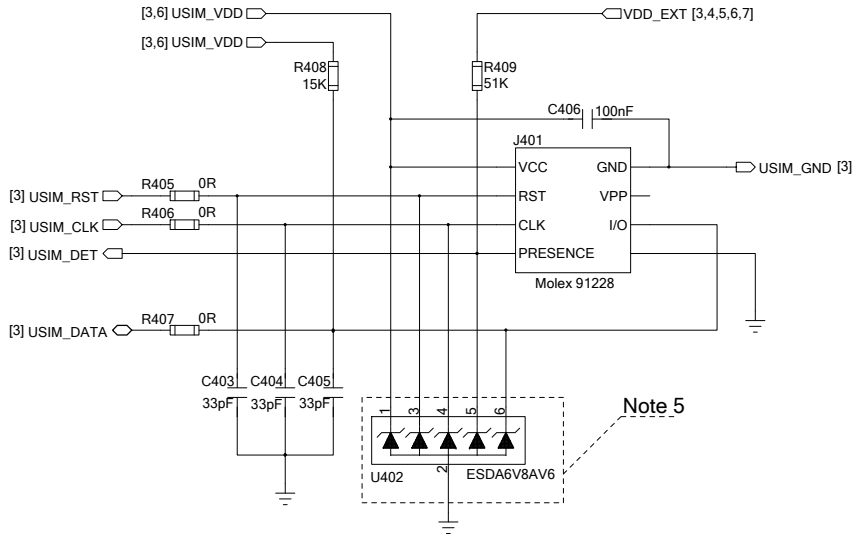
USB Design



Notes:

1. The junction capacitance of the ESD protection devices should be less than 2pF.
2. It is important to route the USB signal traces as differential pairs with ground surrounded. The impedance of USB differential trace is 90Ω.

(U)SIM Design



Notes:

1. R405~R407 are applied to facilitate debugging. It is recommended to reserve the series resistors for (U)SIM signals of the module.
2. R408 can improve anti-jamming capability of the (U)SIM circuit.
3. BG95 supports (U)SIM card hot-plugging, which can be implemented through USIM_DET.
4. The value of C406 should be less than 1μF.
5. Parasitic capacitance of the ESD array should not exceed 15pF.
6. If the system ground plane is complete, USIM_GND can be connected to the system ground directly.

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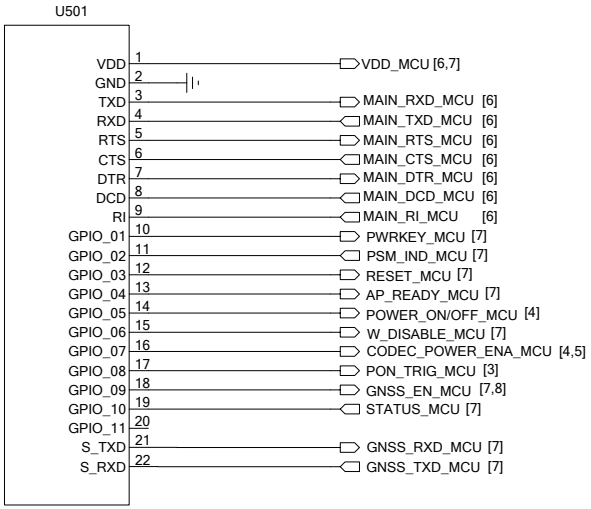
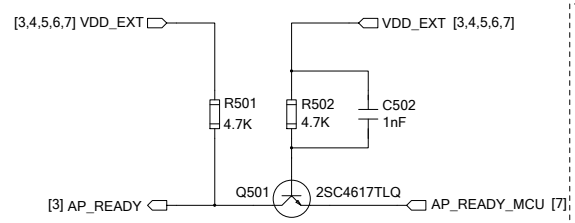
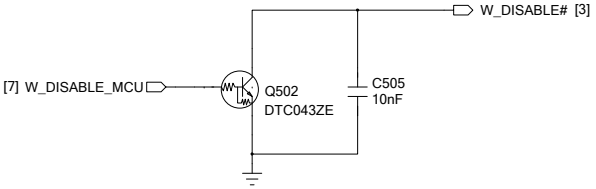
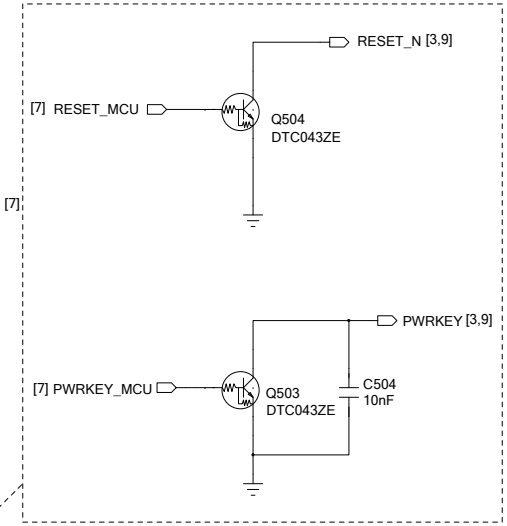
MCU Interfaces



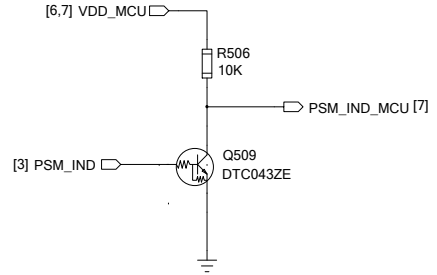
Notes:
1. U501 represents customer's MCU.
2. Please pay attention to the UART connection of RTS/CTS.
3. When BG95 module enters PSM, please set MCU's UART port into the high-impedance mode.



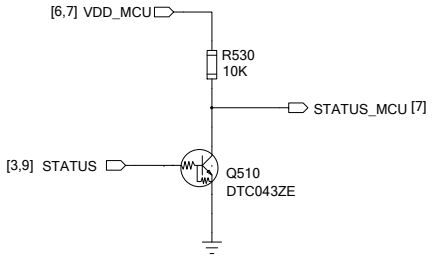




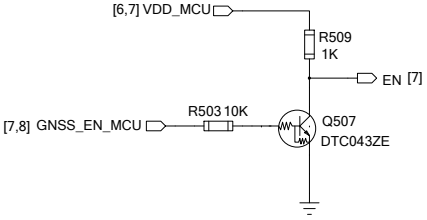
Note 1

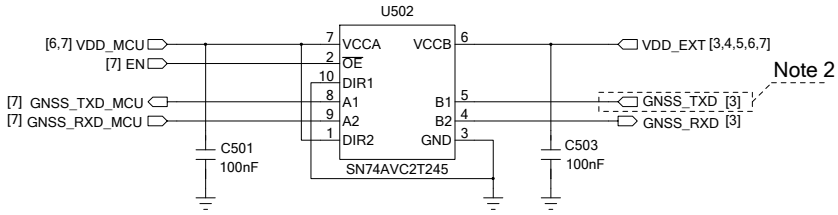


PSM Mode	PSM_IND	PSM_IND_MCU
Y	0	1
N	1	0



State	STATUS	STATUS_MCU
POWER OFF	0	1
POWER ON	1	0





Note 2

Notes:
1. The module can be reset by driving RESET_N to a low level voltage for a duration between 2s and 3.8s.
   The module can be turned on by driving the PWRKEY pin to a low level voltage for a duration between 500ms and 1000ms.
   The module can be turned off by driving the PWRKEY pin to a low level voltage for a duration between 650ms and 1500ms.
2. GNSS_TXD is a BOOT_CONFIG pin. It should not be pulled up before startup.

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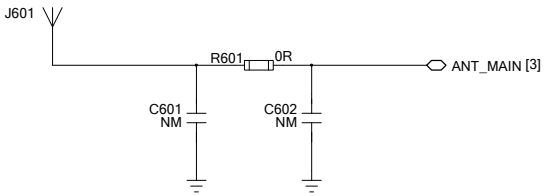
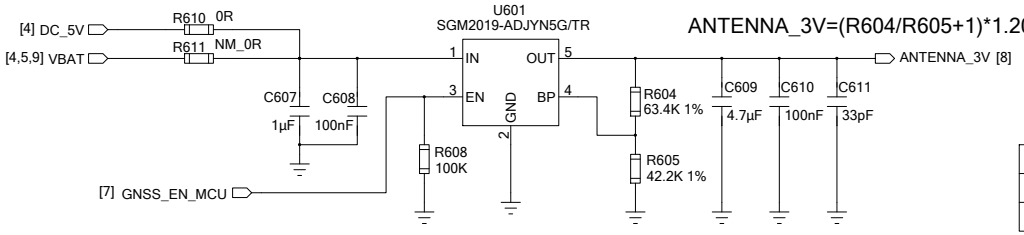
Antenna Interface Designs

Main Antenna Interface



Power Supply for Antenna

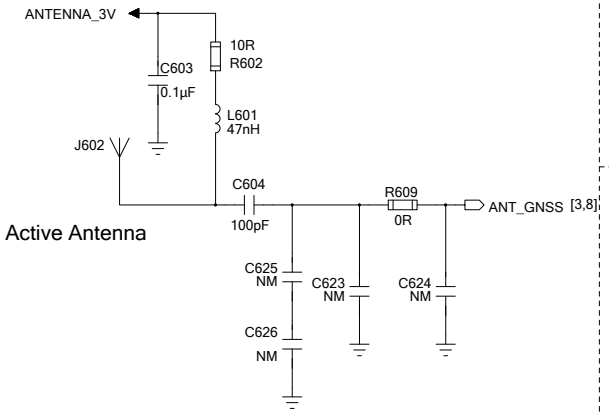


	R610	R611
Standard Solution	Mount	NM
Battery Solution	NM	Mount

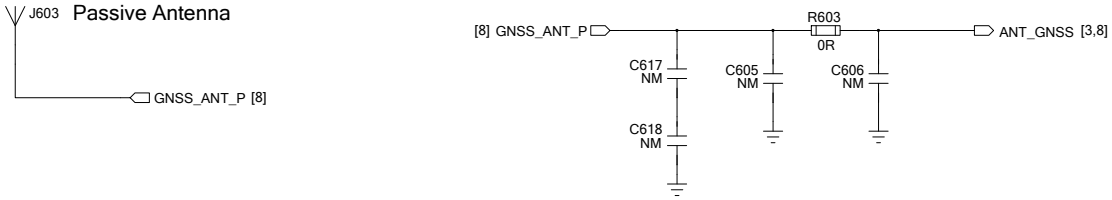
GNSS Antenna Interface

GPS_ENABLE — GPS_EXT — TP601

Active Antenna Design

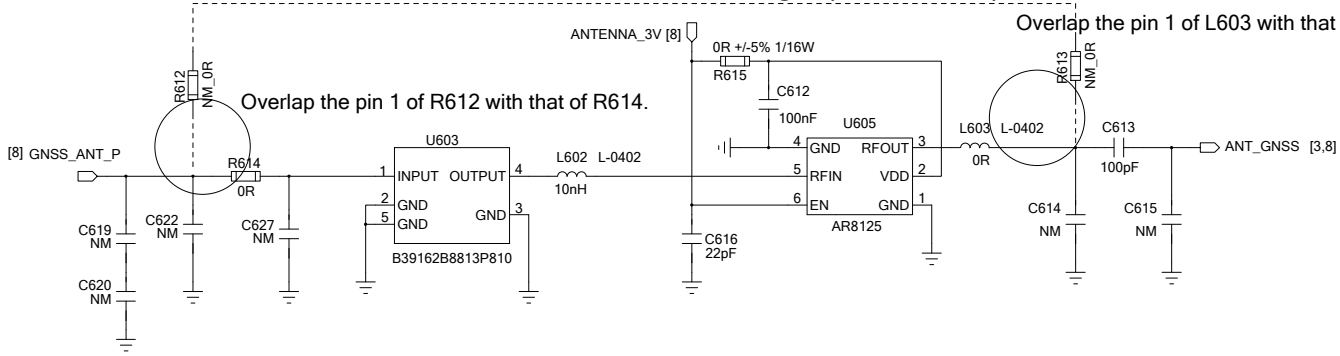


Passive Antenna Design (Solution 1)



The solution is ideal for compact-sized applications where the cable insertion loss from the module to the antenna is small.

Passive Antenna Design (Solution 2)



The solution is ideal for applications where the cable insertion loss from the module to the antenna is large and external LNA and SAW are needed.

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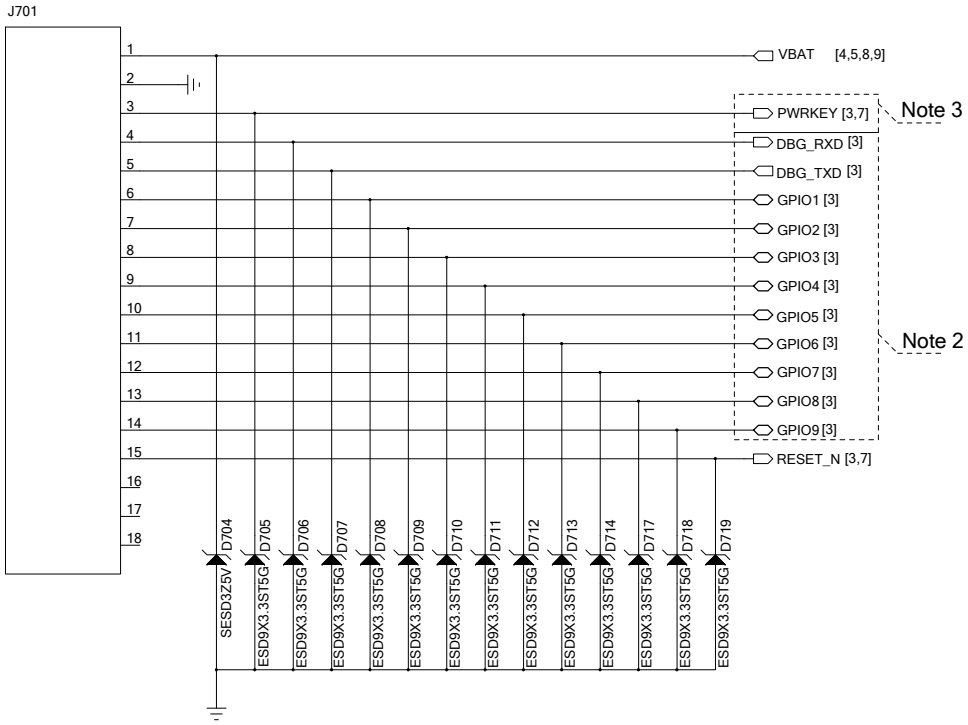
Test Points and Indicators

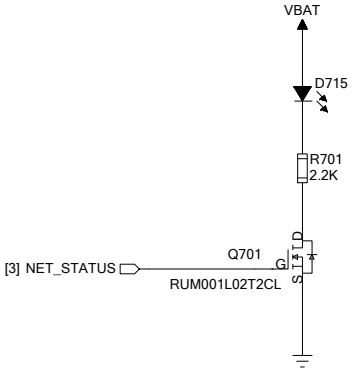
Reserved Test Points

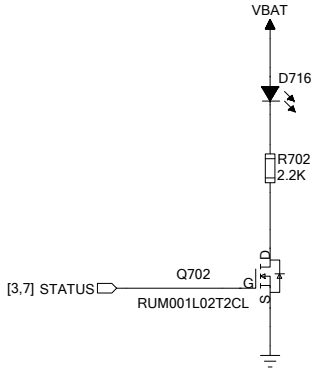


Notes:

1. It is recommended to reserve the test points for debug UART for future software debugging.
2. The voltage level of debug UART and GPIO interfaces is 1.8V. Do not connect them directly to a 3.3V level.
3. PWRKEY should never be pulled down to GND permanently.

Indicators





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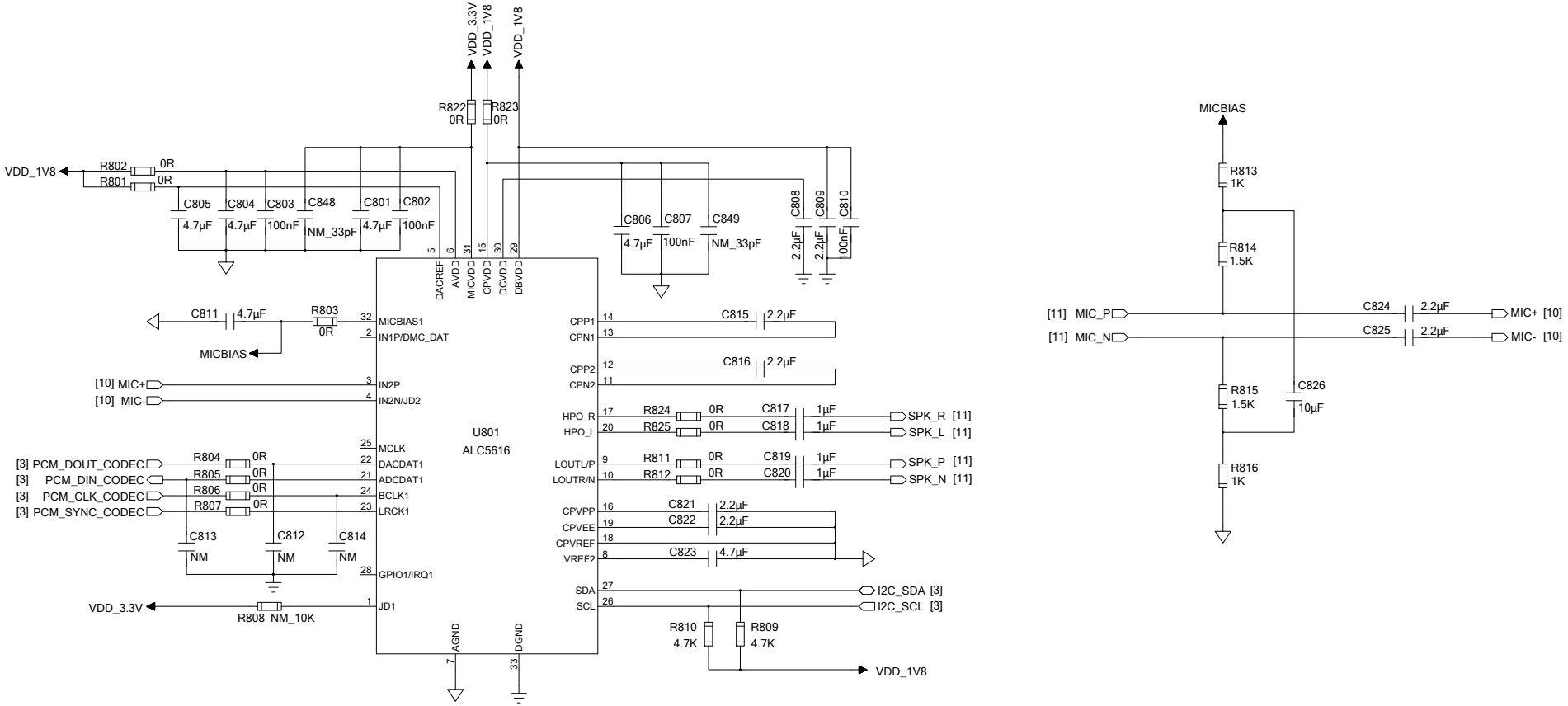
Audio Codec Design



Notes:

1. To ensure that ALC5616 works normally, please follow the power-on and power-off sequences of its power supply.
   Power-on Sequence: power on DBVDD/AVDD/DACREF/CPVDD first, and then MICVDD.
   Power-off Sequence: power off MICVDD first, and then DBVDD/AVDD/DACREF/CPVDD.
   For more details, please refer to ALC5616 datasheet.
2. BG95 module will automatically initialize the codec via I2C interface after it is turned on successfully, so all power supplies for the codec need to be switched on before that.

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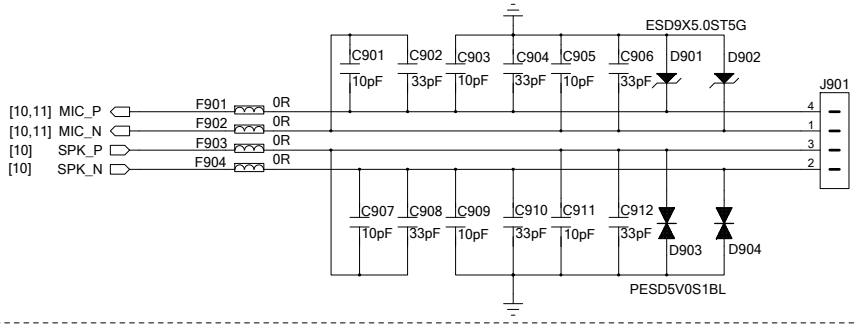
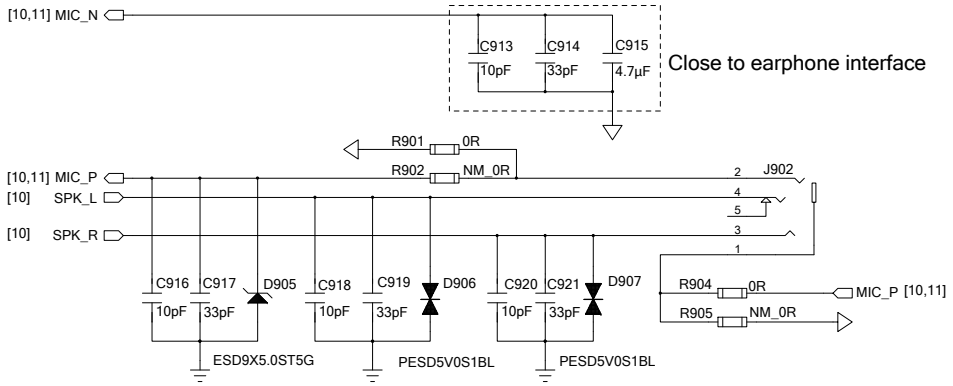
Audio Interface

Handset Application



Earphone Application



	CTIA	OMTP
R902/R905	NM	Mount
R901/R904	Mount	NM

Notes:

1. The analog output only drives earphone and handset. For larger-power loads such as speakers, an audio power amplifier needs to be added in the design.
2. The maximum capacitive loading for speaker is 330pF and that for microphone is 250pF.
3. In handset applications, both the microphone and speaker signal traces need to be routed as differential pairs.
4. In earphone applications, the microphone signal traces need to be routed as differential pairs.
5. All microphone and speaker signal traces should be routed with ground surrounded and far away from noise signals such as clock and DC-DC signals, etc.

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