LG77L (C)
Hardware Design

GNSS Module Series

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Status: Released

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Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service, or repair of any terminal or mobile incorporating the module. Manufacturers of the terminal should notify users and operating personnel of the following safety precautions by incorporating them into all product manuals. Otherwise, Quectel assumes no liability for customers' failure to comply with these precautions.

	Ensure that the product may be used in the country and the required environment, as well as that it conforms to the local safety and environmental regulations.
	Keep away from explosive and flammable materials. The use of electronic products in extreme power supply conditions and locations with potentially explosive atmospheres may cause fire and explosion accidents.
	The product must be powered by a stable voltage source, and the wiring shall conform to security precautions and fire prevention regulations.
	Proper ESD handling procedures must be followed throughout the mounting, handling and operation of any devices and equipment that incorporate the module to avoid ESD damages.

About the Document

Document Information	
Title	**LG77L (C) Hardware Design**
Subtitle	GNSS Module Series
Document Type	Hardware Design
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Revision History

Version	Date	Description
-	2020-09-01	Creation of the document
1.0	2021-01-05	First official release
1.1	2021-07-16	1. Completely reorganized the structure of the document. 2. Added LG77L (B) and LG77L (C). 3. Added Chapters 1.5, 1.6, 1.7, 3.4, 3.5, 5.2.2, 5.3 and 9. 4. Updated the power consumption, sensitivity, 1PPS signal accuracy, and maximum altitude values of LG77L (A) (Table 3). 5. Updated the name of pin 13 from FORCE_ON to WAKEUP. 6. Updated the pin 10 from RESERVED to 3D_FIX. 7. Updated the pin 28 from RESERVED to JAM_IND. 8. Updated the description of the 1PPS (Chapter 4.1.4). 9. Updated the reset sequence (Chapter 4.2.2). 10. Optimized the antenna interface reference designs (Chapter 5.2). 11. Updated the recommended total gain of active antenna into 35 dB (Chapter 5.2.1). 12. Updated the recommended operating conditions (Chapter 6.2). 13. Updated the packaging specifications (Table 12). 14. Updated the notes about module storage (Chapter 8.2). 15. Updated the recommended peak reflow temperature and the reflow time in reflow zone (Chapter 8.3).

Version	Date	Description
1.2	2023-09-04	1. Selected pin name has been updated to agree with a common naming convention across Quectel GNSS modules. The pin has the same physical hardware but with updated name: Pin 34: from ANT_OK to ANT_SHORT. 2. Added the number of current GNSS (*Table 2*). 3. Updated the power consumption data and the sensitivity *(Table 3*). 4. Added chapter of firmware upgrade (*Chapter 1.10*). 5. Added the DC characteristics of all pins (*Table 6*). 6. Updated the reference circuit for V_BCKP (*Chapter 3.2.2*). 7. Added chapter of WAKEUP (*Chapter 4.2.1*) 8. Updated the active antenna reference design with and without antenna status detection (*Figure 18* and *Figure 19*). 9. Updated the maximum input power at RF_IN (*Table 10*). 10. Added the high-level input voltage range for RESET_N (*Table 11*). 11. Added chapter of supply current requirement (*Chapter 6.3*). 12. Updated the packaging information (*Chapter 8.1*). 13. Updated the recommended ramp-to-soak, ramp-up and cool-down slopes (*Figure 28* and *Table 15*).
1.3	2024-07-05	1. Deleted the following EOL products: LG77L (A) and LG77L (B). 2. Updated the tolerances of module's length and width (*Table 2* and *Figure 22*). 3. Moved the C/N0 information in Antenna Selection Guide and Coexistence with Cellular Systems to Quectel_GNSS_Antenna_Application_Note. 4. Updated the inductance of L1 for active antenna with antenna status detection (*Figure 19*). 5. Added the notes specifying that mercury-containing materials and corrosive gases should be avoided for module processing (*Chapter 8.3*).

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1 Product Description

1.1. Overview

The Quectel LG77L (C) supports multiple global positioning and navigation systems: GPS, GLONASS, Galileo, BDS and QZSS. The module also supports SBAS (including WAAS, EGNOS, MSAS and GAGAN) and AGNSS functions.

Key features:

- Single-band, multi-constellation GNSS module with a high-performance and highly reliable positioning engine. This module enables fast and precise GNSS positioning capabilities.
- Integrated RTC.
- Supported serial communication interfaces: UART and I2C.
- Incorporates embedded low-power algorithms designed for different application scenarios.
- Supports multiple power-saving modes, such as Standby, Backup, Periodic and GLP modes.
- Features signalling for active antenna detection and short-circuit protection (when using the suggested peripheral circuits).
- Embedded flash memory provides the capacity for storing user-specific configurations and future firmware updates.

The LG77L (C) module is SMD module with a compact form factor of 7.0 mm × 7.0 mm × 2.0 mm. It can be embedded in your applications through 43 LGA pins.

The module is fully compliant with the EU RoHS Directive.

1.1.1. Special Mark

Table 1: Special Mark

Mark	Definition
●	The symbol indicates that a function or technology is supported by the module(s).

1.2. Features

Table 2: Product Features

Features		LG77L (C)
Grade	Industrial	●
	Automotive	-
Category	Standard Precision GNSS	●
	High Precision GNSS	-
	DR	-
	RTK	-
	Timing	-
VCC Voltage	2.8–4.3 V, Typ.: 3.3 V	●
V_BCKP Voltage	2.0–4.3 V, Typ.: 3.3 V	●
I/O Voltage [1]	Typ.: 1.8 V or 2.8 V	●
Communication Interfaces	UART	●
	SPI	-
	I2C [2]	●
	CAN	-
	USB	-
Integrated Features	Additional LNA	-
	Additional Filter	●
	RTC crystal	●
	TCXO oscillator	●
	6-axis IMU	-
Constellations and Frequency Bands	Number of Concurrent GNSS	3 + QZSS

[1] It depends on the voltage domain of VCC_IO.
[2] I2C interface is supported only on firmware versions ending with “SC”.

Features			LG77L (C)
	GPS	L1 C/A	●
		L5	-
		L2C	-
	GLONASS [3]	L1	●
		L2	-
	Galileo [3]	E1	●
		E5a	-
		E5b	-
	BDS [3]	B1I	●
		B2a	-
		B2I	-
	QZSS	L1 C/A	●
		L5	-
		L2C	-
	NavIC	L5	-
SBAS		L1	●
Temperature Range	Operating temperature range		-40 °C to +85 °C
	Storage temperature range		-40 °C to +90 °C
Physical Characteristics	Size		(7.0 +0.30/-0.15) mm × (7.0 +0.30/-0.15) mm × (2.0 ±0.2) mm
	Weight		Approx. 0.2 g

NOTE

For more information about GNSS constellation configuration, see *document [1] protocol specification*.

[3] LG77L (C) cannot support BDS and GLONASS/Galileo at the same time.

1.3. Performance

Table 3: Product Performance

Parameter	Specification	LG77L (C)
Power Consumption [4] (GPS + GLONASS)	Acquisition	24 mA (79.2 mW)
	Tracking	23 mA (75.9 mW)
	Standby Mode	0.9 mA (2.97 mW)
	Backup Mode	6 μA (19.8 μW)
Sensitivity [4] (GPS + GLONASS)	Acquisition	-146 dBm
	Reacquisition	-156 dBm
	Tracking	-163 dBm
TTFF [5] (with EASY)	Cold Start	17 s
	Warm Start	5 s
	Hot Start	2 s
TTFF (with EPO)	Cold Start	8 s
	Warm Start	6 s
	Hot Start	2 s
TTFF [4] (without AGNSS)	Cold Start	25 s
	Warm Start	23 s
	Hot Start	2 s
Horizontal Position Accuracy [6]		2.5 m
Update Rate		Default: 1 Hz; Max. 10 Hz
Accuracy of 1PPS Signal [4]	RMS	50 ns
Velocity Accuracy [4]	Without aid	0.1 m/s

[4] Room temperature, all satellites at -130 dBm.
[5] Open-sky, active high precision GNSS antenna.
[6] CEP, 50 %, 24 hours static, -130 dBm, more than 6 SVs.

Parameter	Specification	LG77L (C)
Acceleration Accuracy [4]	Without aid	0.1 m/s²
Dynamic Performance [4]	Maximum Altitude	10000 m
	Maximum Velocity	515 m/s
	Maximum Acceleration	4g

1.4. Block Diagram

A block diagram of the module is presented below. It includes a single-chip GNSS IC, a front-end section with an additional SAW filter, a TCXO and a XTAL.

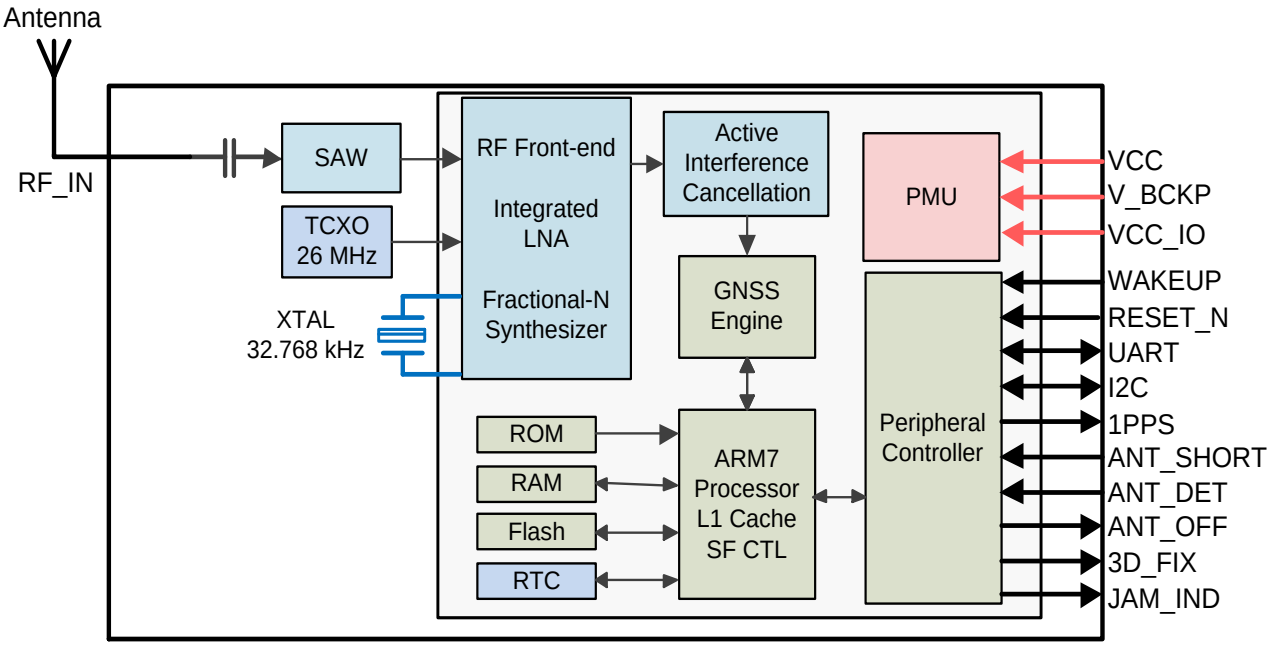


Figure 1: Block Diagram

1.5. GNSS Constellations and Frequency Bands

The module is single-band GNSS receivers that can receive and track concurrently multiple GNSS constellations. Owing to their RF front-end architecture, they can track the following GNSS constellations: GPS, GLONASS, Galileo, BDS and QZSS plus SBAS satellites. If low power consumption is a key factor, the module can be configured to track a specific subset of GNSS constellations.

QZSS is a regional navigation satellite system that transmits signals compatible with the GPS L1 C/A, L1C, L2C and L5 signals for the Pacific region, including Japan and Australia. The modules can detect and track QZSS L1 C/A signal concurrently with GPS signals, leading for better signal availability especially under challenging conditions, e.g., in dense urban areas.

Table 4: GNSS Constellations and Frequency Bands

System	Signals
GPS	L1 C/A: 1575.42 MHz
GLONASS	L1: 1602 MHz + K × 562.5 kHz, K= (-7 to +6, integer)
Galileo	E1: 1575.42 MHz
BDS	B1I: 1561.098 MHz
QZSS	L1 C/A: 1575.42 MHz

NOTE

LG77L (C) cannot support BDS and GLONASS/Galileo at the same time.

1.6. Augmentation System

1.6.1. SBAS

The module supports the reception of SBAS signals. By augmenting primary GNSS constellations with additional satellite-broadcast messages, the system improves the accuracy and reliability of GNSS information by correcting signal measurement errors and providing information about signal accuracy, integrity, continuity and availability. SBAS transmits signals for ranging or distance measurement, thus further improving availability. Supported SBAS systems: WAAS, EGNOS, MSAS and GAGAN.

1.7. AGNSS

The modules support AGNSS feature that significantly reduces the module's TTFF, especially under lower signal conditions. To implement the AGNSS feature, the module should get the assistance data including the current time and rough position. For more information, see *document [2] AGNSS application note*.

1.7.1. EASY

The module supports the EASY technology to improve TTFF. To achieve that goal, the EASY technology provides ancillary information, such as ephemeris and almanac.

The EASY technology works as an embedded software to accelerate TTFF by predicting satellite orbit messages from the received ephemeris. After receiving the broadcast ephemeris for the first time, the module automatically calculates and predicts the orbit information up to the subsequent 3 days, and saves the predicted information in the internal memory. The module will use the information for positioning if there is not enough information from satellites, resulting in improved positioning and TTFF.

The EASY function can reduce TTFF to 5 s in a warm start. In this case, the backup domain should still be valid. To obtain enough broadcast ephemeris information from GNSS satellites after fixing the position, the GNSS module should keep tracking the information for at least 10 minutes in strong-signal environments.

The EASY function is enabled by default, and can be disabled with **$PMTK869**. For more information, see *document [1] protocol specification*.

1.7.2. EPO

The modules feature a leading AGNSS technology known as EPO, which significantly reduces the TTFF for up to 14 days. For more information about EPO, see *document [2] AGNSS application note*.

1.8. LOCUS

The modules support the LOCUS embedded logger function, which allows users to accurately analyze satellite navigation data. When enabled, it automatically logs position information to the internal flash memory. As a result, module power consumption is reduced eliminating the need for continuous reception of NMEA messages. The modules provide more than 16 hours of log capacity (64 KB). The current status of the LOCUS function may be queried with **$PMTK183**. For more information about the command, see *document [1] protocol specification*.

1.9. Multi-tone AIC

The module features a function called multi-tone active interference cancellation (AIC) to decrease harmonic distortion of RF signals from Wi-Fi, Bluetooth, and 2G, 3G, 4G and 5G networks.

Up to 12 AIC tones embedded in the module provide effective narrow-band interference and jamming elimination. Thus, the GNSS signal could be demodulated from the jammed signal, which can ensure better navigation quality.

The AIC function is enabled by default, and it can be disabled by **$PMTK286**. For more information about the command, see *document [1] protocol specification*.

The anti-jamming performance of the AIC is illustrated in the following figure:

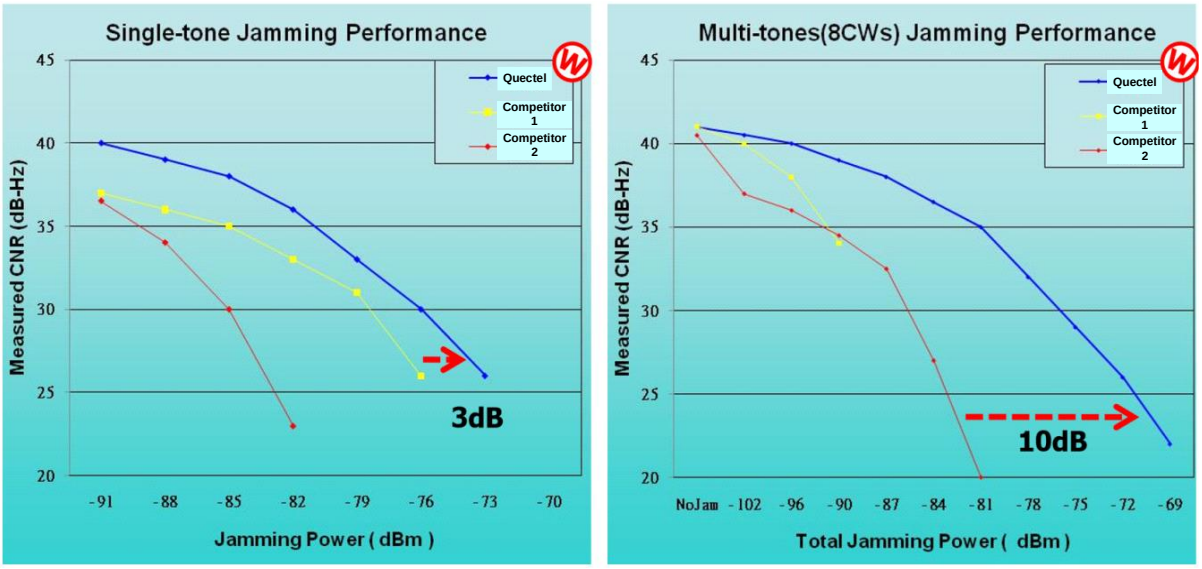


Figure 2: Anti-Jamming Performance with AIC

1.10. Firmware Upgrade

The module is delivered with preprogrammed firmware. Quectel may periodically release firmware versions that contain bug fixes or offer performance optimizations. It is highly important to implement a firmware upgrade mechanism in your system. A firmware upgrade is the process of transferring a binary file image to the receiver and storing it in non-volatile flash. For more information, see *document [3] firmware upgrade guide*.

2 Pin Assignment

The Quectel LG77L (C) is equipped with 43 LGA pins by which they can be mounted on your PCB.

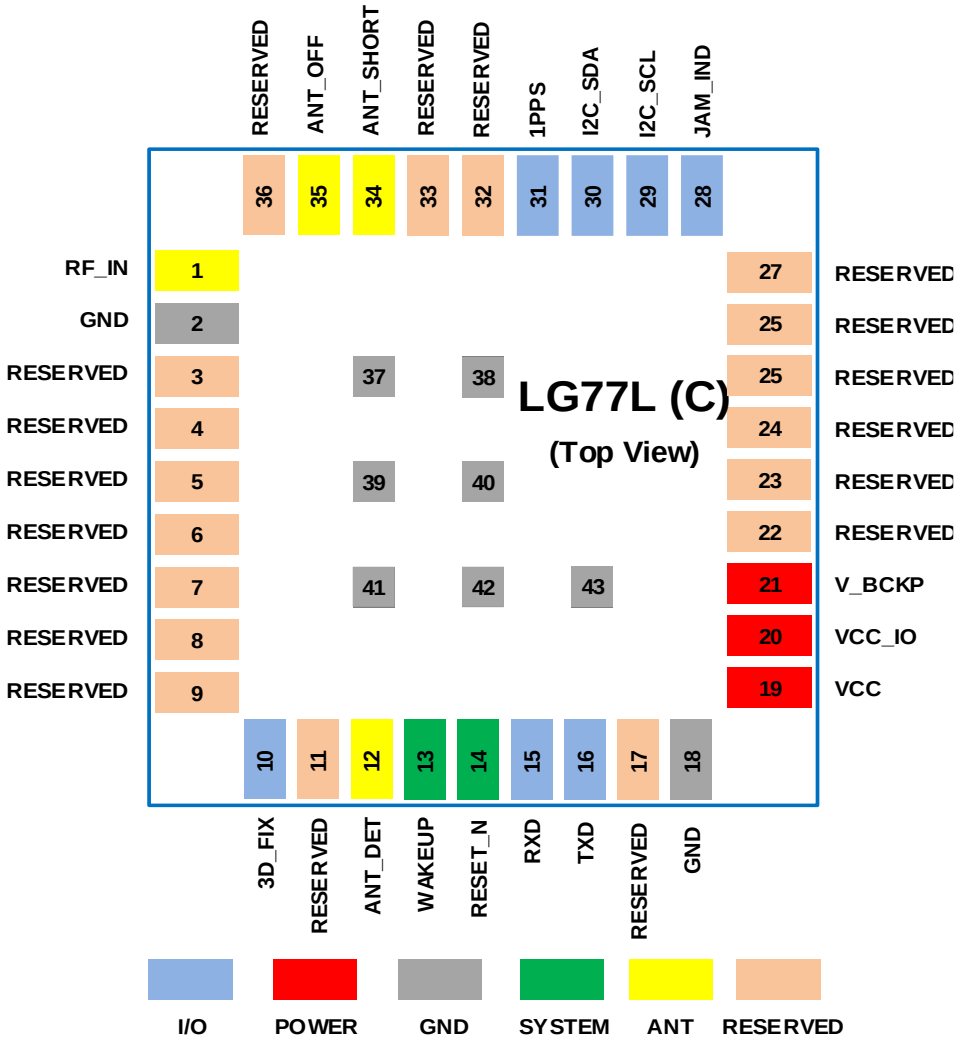


Figure 3: Pin Assignment

Table 5: I/O Parameter Definition

Type	Description
AI	Analog Input
DI	Digital Input
DIO	Digital Input/Output
DO	Digital Output
PI	Power Input

Table 6: Pin Description

Function	Name	No.	I/O	Description	DC Characteristics	Remarks
Power	VCC	19	PI	Main power supply	Vmax = 4.3 V Vmin = 2.8 V Vnom = 3.3 V	Requires clean and steady voltage.
	V_BCKP	21	PI	Backup power supply for RTC domain	Vmax = 4.3 V Vmin = 2.0 V Vnom = 3.3 V	V_BCKP must be connected to power supply for startup, and it should always be powered if hot (warm) start is needed.
	VCC_IO	20	PI	Digital I/O port power supply	**1.8 V I/O voltage:** Vmax = 1.98 V Vmin = 1.62 V Vnom = 1.8 V **2.8 V I/O voltage:** Vmax = 3.08 V Vmin = 2.52 V Vnom = 2.8 V	Powered by an external power supply. Powers I/O pins and determines their power domain.
I/O	TXD	16	DO	Transmits data	V_{OL}min = -0.3 V V_{OL}max = 0.15 V × VCC_IO V_{OH}min = 0.85 V × VCC_IO V_{OH}max = 3.6 V V_{OH}nom = VCC_IO	The UART interface supports standard NMEA, PMTK and PQ messages and firmware upgrade.
	RXD	15	DI	Receives data	V_{IL}min = -0.3 V V_{IL}max = 0.25 V × VCC_IO V_{IH}min = 0.75 V × VCC_IO	

Function	Name	No.	I/O	Description	DC Characteristics	Remarks
					V_{IH}max = VCC_IO + 0.3 V V_{IH}nom = VCC_IO	
	I2C_SCL	29	DI	I2C serial clock	V_{IL}min = -0.3 V V_{IL}max = 0.25 V × VCC_IO V_{IH}min = 0.75 V × VCC_IO V_{IH}max = VCC_IO + 0.3 V V_{IH}nom = VCC_IO	The I2C interface supports standard NMEA, PMTK and PQ messages. If unused, leave the pins N/C (not connected).
	I2C_SDA	30	DIO	I2C serial data	V_{OL}min = -0.3 V V_{OL}max = 0.15 V × VCC_IO V_{OH}min = 0.85 V × VCC_IO V_{OH}max = 3.6 V V_{OH}nom = VCC_IO	
	3D_FIX	10	DO	3D fix indication	V_{OL}min = -0.3 V V_{OL}max = 0.15 V × VCC_IO V_{OH}min = 0.85 V × VCC_IO V_{OH}max = 3.6 V V_{OH}nom = VCC_IO	Active high. If unused, leave the pin N/C.
	JAM_IND	28	DO	Jamming indication		Active low. If unused, leave the pin N/C.
	1PPS	31	DO	One pulse per second		Synchronized on rising edge. If unused, leave the pin N/C.
ANT	RF_IN	1	AI	GNSS antenna interface	-	50 Ω characteristic impedance.
	ANT_DET	12	DI	Active antenna open-circuit detection	V_{IL}min = -0.3 V V_{IL}max = 0.25 V × VCC_IO V_{IH}min = 0.75 V × VCC_IO V_{IH}max = VCC_IO + 0.3 V V_{IH}nom = VCC_IO	If unused, leave the pin N/C.
	ANT_SHORT	34	DI	Active antenna short-circuit detection		
	ANT_OFF	35	DO	Active antenna power control	V_{OL}min = -0.3 V V_{OL}max = 0.15 V × VCC_IO V_{OH}min = 0.85 V × VCC_IO V_{OH}max = 3.6 V V_{OH}nom = VCC_IO	
System	WAKEUP	13	DI	Wakes up the module from the Backup mode	V_{IL}min = -0.3 V V_{IL}max = 0.275 V V_{IH}min = 0.825 V V_{IH}max = 1.4 V	Active high Leave this pin N/C or at low level before entering the Backup

Function	Name	No.	I/O	Description	DC Characteristics	Remarks
						mode. If unused, leave the pin N/C.
	RESET_N	14	DI	Resets the module	V_{IL}min = -0.3 V V_{IL}max = 0.25 V × VCC_IO V_{IH}min = 0.75 V × VCC_IO V_{IH}max = VCC_IO + 0.3 V V_{IH}nom = VCC_IO	Active low.
GND	GND	2, 18, 37–43	-	Ground	-	Ensure a good GND connection to all GND pins of the module, preferably with a large ground plane.
RESERVED	RESERVED	3–9, 11, 17, 22–27, 32, 33, 36	-	Reserved	-	These pins must be left N/C and cannot be connected to power or GND.

NOTE

Leave RESERVED and unused pins N/C.

3 Power Management

The module features a power optimized architecture with built-in autonomous energy saving capabilities to minimize power consumption at any given time. The receive can be used in five operating modes: Standby mode, Periodic mode, GLP mode, and Backup mode for optimum power consumption, and Continuous mode for optimum performance.

3.1. Power Unit

VCC is the supply voltage pin of the module. It supplies the PMU which in turn supplies the entire system. The load current of the VCC pin varies according to VCC voltage level, processor load and satellite acquisition. It is important to supply sufficient current and make sure the power supply is clean and stable.

The V_BCKP pin supplies the backup domain, which includes RTC and low power RAM. To achieve quick startup and improve TTFF, the backup domain power supply should be valid at all times during Backup mode. If the VCC is not valid, the V_BCKP supplies low power RAM that contains all the necessary GNSS data and some of the user configuration variables.

The VCC_IO pin supplies power for the digital I/O pins of module.

The module's internal power supply is shown below:

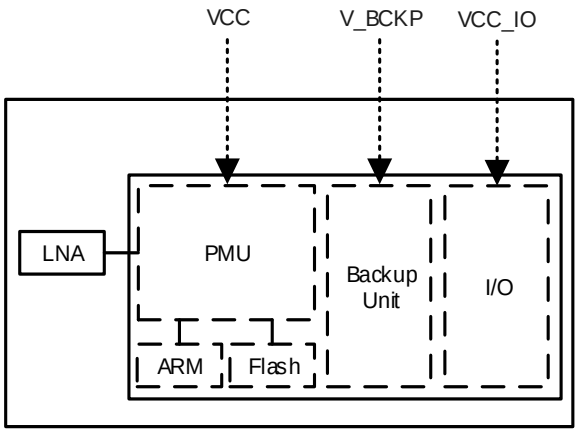


Figure 4: Internal Power Supply

NOTE

The V_BCKP pin must be powered for the module to start up and work normally. Its supply voltage range is 2.0–4.3 V.

3.2. Power Supply

3.2.1. VCC

The VCC is the supply voltage pin that supplies BB and RF.

Module power consumption may vary by several orders of magnitude, especially when power saving mode is enabled. Therefore, it is important for the power supply to be able to sustain peak power for a short time, ensuring that load current does not exceed the rated value. When the module starts up or switches from the Backup mode to the Continuous mode, VCC must charge the internal capacitors in the core domain, which can result in a significant current drain.

For low-power applications that use power saving mode, it is important for the LDO at power supply or module input to be able to provide sufficient current when the module is switched from the Backup mode to the Continuous mode. An LDO with a high PSRR should be chosen for good performance. In addition, a TVS, and a combination of a10 µF, a 100 nF and a 33 pF decoupling capacitor should be added near the VCC pin. The minimum value capacitor should be placed the closest to the VCC pin.

It is not recommended to use a switching DC-DC power supply.

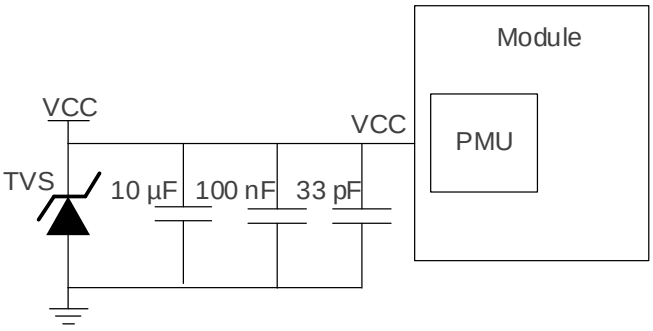


Figure 5: VCC Input Reference Circuit

NOTE

Ensure the module VCC is controlled by MCU to save power or restart the module if it enters an abnormal state.

3.2.2. V_BCKP

The V_BCKP pin supplies power for the backup domain. Use of valid time and GNSS orbit data at startup allows GNSS hot (warm) start. V_BCKP must be connected to power supply for startup, and it should always be powered if hot (warm) start is needed.

If there is a constant power supply in your system, it can be used to provide a suitable voltage to power V_BCKP.

It is recommended to place a TVS and a combination of a 4.7 µF, a 100 nF and a 33 pF capacitor and a bead near the V_BCKP pin. The figure below illustrates the reference design for powering the backup domain.

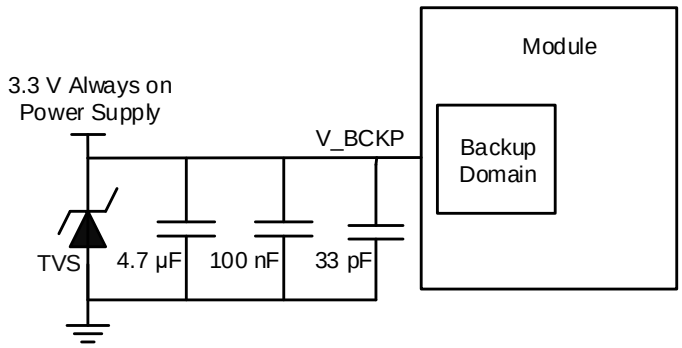


Figure 6: Backup Domain Input Reference Circuit

V_BCKP can also be powered by a 3.7 V lithium battery. It is recommended to control the enable pin of LDO via MCU, as shown below.

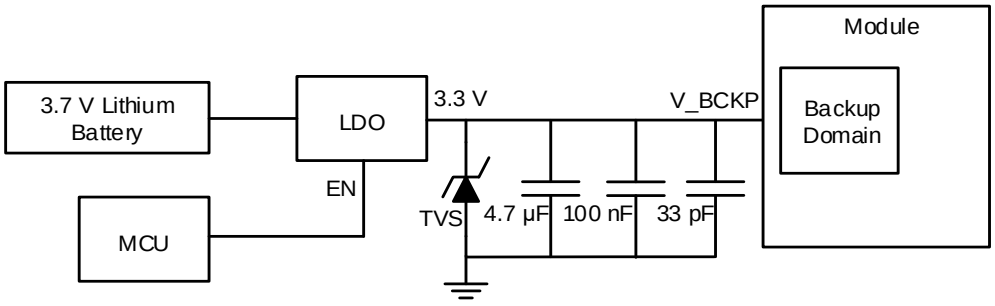


Figure 7: Reference Power Supply Circuit with 3.7 V Lithium Battery

NOTE

1. If V_BCKP is below the minimum value of the recommended operating voltage, the module cannot work normally.
2. It is recommended to control the module V_BCKP via MCU to restart the module if the module enters an abnormal state.

3.2.3. VCC_IO

The VCC_IO pin can be directly powered by an external power supply, or it can be supplied from VCC after a voltage level conversion. The voltage level conversion circuit using an LDO is shown in the figure below.

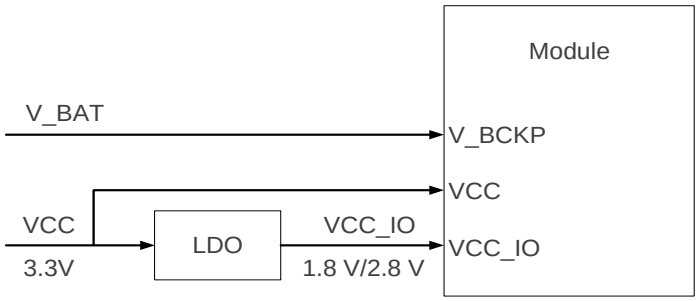


Figure 8: VCC to VCC_IO Reference Circuit

3.3. Power Modes

3.3.1. Feature Comparison

The module features supported in different modes are listed in the table below.

Table 7: Feature Comparison in Different Power Modes

Features	Continuous	Standby	Backup	Periodic	GLP
NMEA from UART	●	-	-	O	●
Antenna Detection	●	-	-	O	●
1PPS	●	-	-	O	●
RF	●	-	-	O	●

Features	Continuous	Standby	Backup	Periodic	GLP
Acquisition & Tracking	●	-	-	**O**	●
Power Consumption	High	Low	Low	Medium	Medium
Position Accuracy	High	-	-	Low	Medium

NOTE

O = Supported in Continuous periodic mode

3.3.2. Continuous Mode

If VCC, V_BCKP and VCC_IO are powered on, the module automatically enters the Continuous mode that comprises acquisition mode and tracking mode. In acquisition mode, the module starts to search for satellites and to determine visible satellites, coarse frequency, as well as the code phase of satellite signals. Once the acquisition is completed, the module automatically switches to tracking mode. In tracking mode, the module tracks satellites and demodulates the navigation data from specific satellites.

3.3.3. Standby Mode

The Standby mode is a power saving mode in which the internal core and the I/O power domain remain active, but the RF is powered off, so the module stops satellite searching and navigation. The UART interface still receives commands or any other data, but NMEA messages cannot be output via the interface. Upon exiting Standby mode, the module uses internal ancillary information such as GPS time, ephemeris, and last position to ensure the fastest possible TTFF during a hot or warm start.

- Enter Standby mode: Send the **$PMTK161**. For more information about the command, see *document [1] protocol specification*.
- Exit Standby mode: Send any data via the UART interface.

3.3.4. Backup Mode

For power-sensitive applications, the module supports a Backup mode to reduce power consumption. In the Backup mode, the module stops acquiring and tracking satellites. The UART is not accessible. But the SRAM memory in the backup domain is active, which contains all the necessary GNSS information for a quick start-up, and a small amount of user configuration variables. Due to the SRAM memory, the EASY technology is available.

If VCC and VCC_IO are cut off and V_BCKP powers the RTC domain, the module switches from continuous mode to backup mode. Only backup domain is active in the Backup mode and it keeps track of time.

There are two ways to enter or exit the Backup mode:

The first way:

- Enter Backup mode: Send **$PMTK225**. For more information on the command, see *document [1] protocol specification*.
- Exit Backup mode: Pull the WAKEUP pin up.

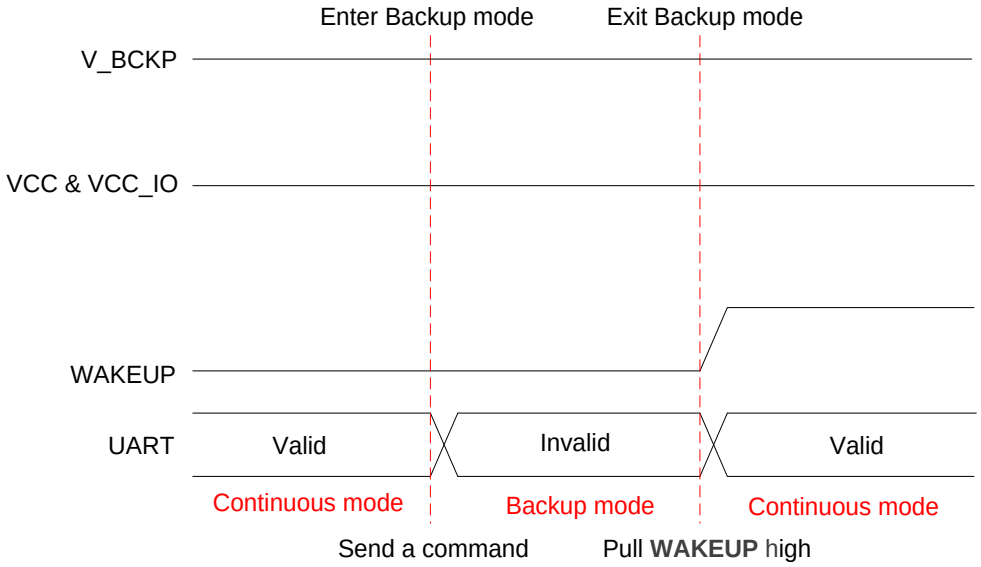


Figure 9: Entering/Exiting Backup Mode Sequence – 1

The second way:

- Enter Backup mode: Cut off the power supply of VCC and VCC_IO while keep V_BCKP powered.
- Exit Backup mode: Restore the VCC and VCC_IO power supply.

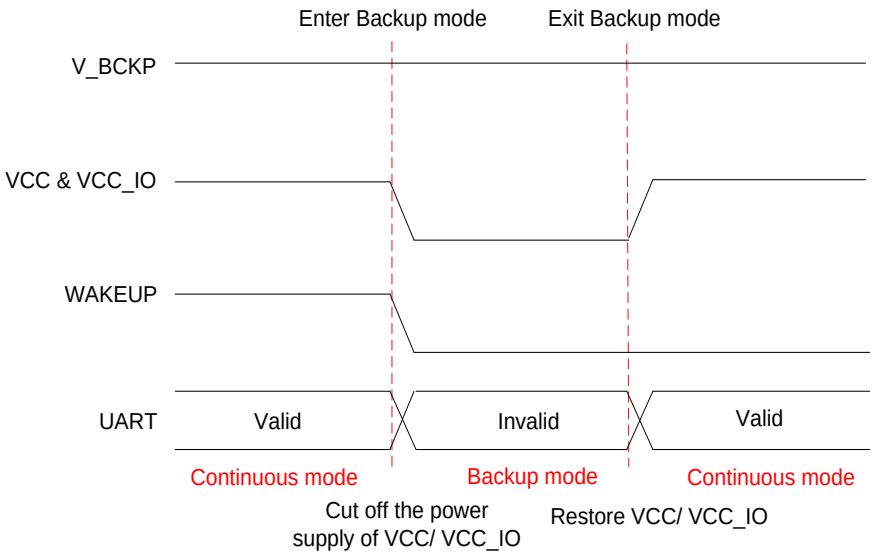


Figure 10: Entering/Exiting Backup Mode Sequence – 2

NOTE

Ensure a stable V_BCKP voltage without rush or drop when the VCC is switched on or off.

3.3.5. Periodic Mode

The Periodic mode includes Periodic standby mode and Periodic backup mode. In Periodic mode, the module switches between the Continuous mode and the Standby/Backup mode periodically to reduce power consumption. The module achieves a balance between positioning accuracy and power consumption; however, its performance is lower than in the Continuous mode. In the Periodic mode, the module power supply should be uninterrupted. You can make the module enter/exit the Periodic mode by sending **$PMTK225**. For more information about the commands, see *document [1] protocol specification*.

The Periodic mode is configured by setting the following parameters: **Run Time**, **Second Run Time**, **Sleep Time**, and **Second Sleep Time** that describe the operating cycle of the Periodic mode functioning. After sending command for entering the Periodic mode, the module first goes into the Continuous mode and remains in it for several minutes. Afterwards, the module enters the Periodic mode and operates according to the above-mentioned parameters set by the PMTK command.

The Periodic mode is illustrated in the following figure. If the module fails to fix the position in **Run Time**, it switches to the **Second Run Time** and **Second Sleep Time** automatically. If it manages to fix the position again, the module will return to **Run Time** and **Sleep Time**.

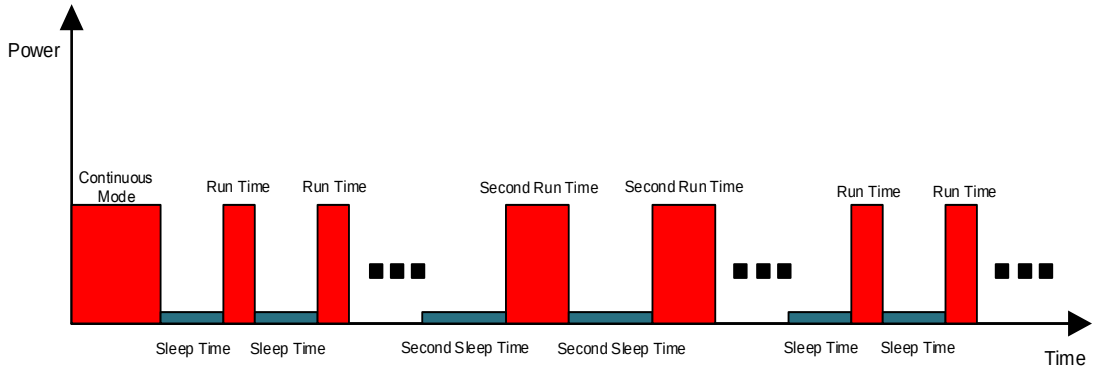


Figure 11: Periodic Mode

The average current value can be calculated with the following formula:

$I_{periodic} = (I_{tracking} \times T1 + I_{standby/backup} \times T2) / (T1 + T2)$

T1 = Run Time, T2 = Sleep Time.

NOTE

1. Before entering the Periodic mode, make sure that the module is in tracking mode. Otherwise, there is a risk of satellite-tracking failure. In weak signal environments, it is recommended to set a longer **Second Run Time** to ensure successful reacquisition.
2. Before entering Periodic Backup mode, make sure that the WAKEUP pin is N/C or at low level; otherwise, Periodic Backup mode will be unavailable.

3.3.6. GLP Mode

The GLP (GNSS Low Power) mode is an optimized solution for wearable fitness trackers. It reduces power consumption by disabling high accuracy positioning.

In the GLP mode, the module achieves good positioning performance while walking or running. In challenging environments, the module automatically switches to the Continuous mode to keep good accuracy. As a result, the module can still achieve maximum performance with the lowest power consumption.

You can set the module to GLP mode or force it to exit the mode with **$PQGLP**. For more information about the commands, see *document [1] protocol specification*.

NOTE

1. Before the module enters GLP mode, set the baud rate to 115200 bps and the frequency to 1 Hz.
2. When the module enters GLP mode, the 1PPS function is disabled. When GLP mode is enabled, the SBAS function cannot be used.
3. In highly dynamic scenarios, the module's positioning accuracy is slightly reduced in GLP mode.
4. In complex environments, the module automatically returns to continuous mode to maintain good positioning accuracy.

3.4. Power-up Sequence

Once the VCC, V_BCKP and VCC_IO are powered up, the module starts up automatically and the voltage should rise rapidly in less than 50 ms.

To ensure the correct power-up sequence, the backup unit should start up no later than the PMU. Hence, the V_BCKP must be powered simultaneously with the VCC or before it.

Ensure that the VCC, V_BCKP and VCC_IO have no rush or drop during rising time, and then keep the voltage stable. The recommended ripple is < 50 mV.

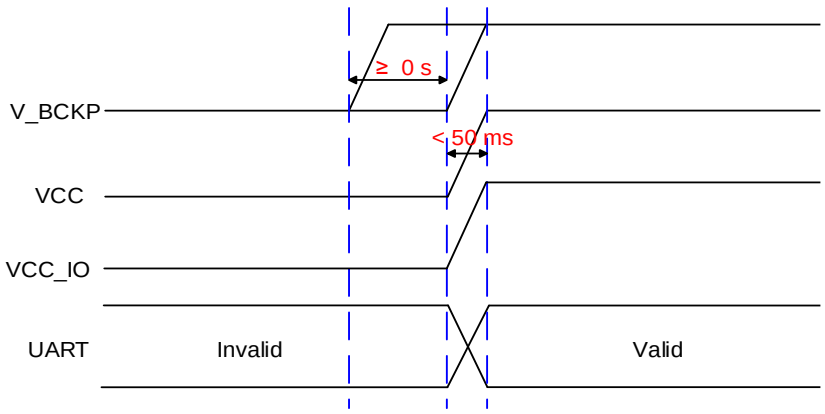


Figure 12: Power-up Sequence

3.5. Power-down Sequence

Once the VCC, V_BCKP and VCC_IO are shut down, the module turns off automatically and the voltage should drop quickly within less than 50 ms. It is recommended to use a voltage regulator that supports fast discharging.

To avoid abnormal voltage conditions, if VCC, V_BCKP and VCC_IO fall below the specified minimum value, the system must initiate a power-on restart by reducing VCC, V_BCKP and VCC_IO to less than 100 mV for at least 1 s.

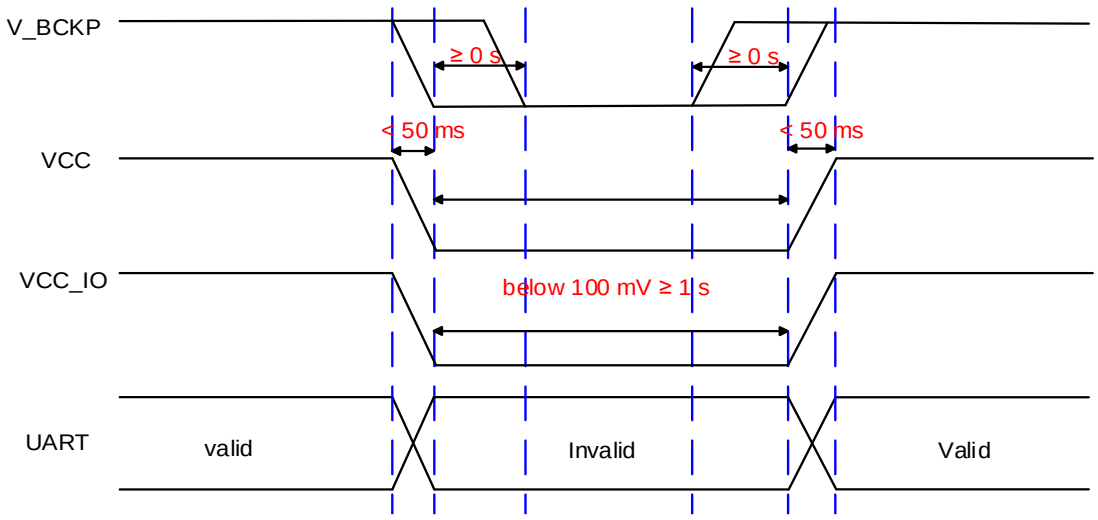


Figure 13: Power-down and Power-on Restart Sequence

4 Application Interfaces

4.1. I/O Pins

4.1.1. Communication Interfaces

The following interfaces can be used for data reception and transmission.

4.1.1.1. UART Interface

The module has one UART interface with the following features:

- Supports standard NMEA, PMTK, PQ messages and firmware upgrade.
- Supported baud rates: 9600 bps, 14400 bps, 19200 bps, 38400 bps, 57600 bps, 115200 bps, 230400 bps, 460800 bps, 921600 bps.
- Hardware flow control and synchronous operation are not supported.

For more information, see *document [1] protocol specification*.

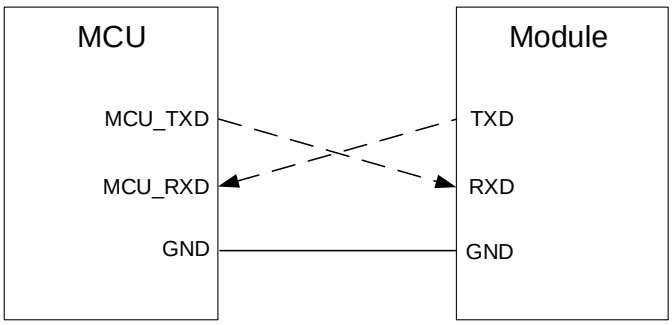


Figure 14: UART Interface Reference Design

A reference design is shown in the figure above. For more information, see *document [4] reference design*.

NOTE

1. UART interface default settings may vary depending on software version. See the relevant software versions for details.
2. If the I/O voltage of MCU does not match the module, a level-shifting circuit must be used.

4.1.1.2. I2C Interface

The module provides one I2C interface with the following features:

- Supports standard NMEA, PMTK and PQ messages.
- Supports fast mode, with bit rates up to 400 kbps.
- Operates as a slave.
- Open-drain output.

For more information, see *document [5] I2C application note*.

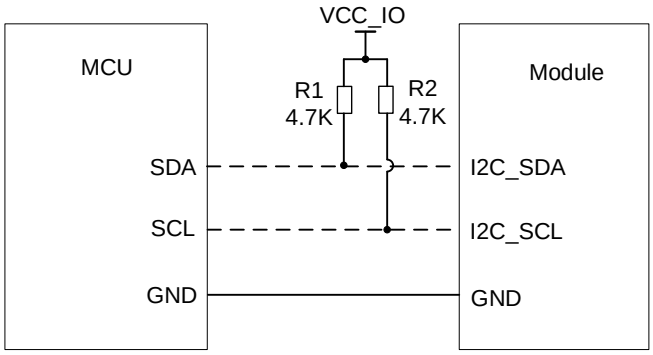


Figure 15: I2C Interface Reference Design

A reference design is shown in the figure above. For more information, see *document [4] reference design*.

NOTE

1. If the I/O voltage of MCU does not match the module, a level-shifting circuit must be used.
2. The I2C interface is supported only on firmware versions ending with “SC”.

4.1.2. 1PPS

The 1PPS output pin can be used for time pulse signals, it generates a one pulse per second periodic signal synchronized to a GNSS time grid with intervals. Maintaining high accuracy of 1PPS requires visible satellites in an open sky environment and powered VCC. See *Table 3: Product Performance* for details about pulse accuracy.

4.1.3. 3D_FIX

The 3D_FIX is assigned as a fix flag output. The pin will output a high voltage level to indicate successful positioning.

4.1.4. JAM_IND

The module provides an indicator pin to detect any jamming that may impact the module. If jamming is detected, the JAM_IND pin outputs a low-level signal; otherwise, it outputs a high-level signal.

4.2. System Pins

4.2.1. WAKEUP

The WAKEUP pin is pulled down internally and it belongs to backup domain. Leave this pin N/C or at low level before entering the Backup mode. The WAKEUP pin can wake up the module from the Backup mode if it is driven to a high voltage level. If unused, leave the pin N/C.

4.2.2. RESET_N

RESET_N is an input pin. The module can be reset by driving the RESET_N low for at least 100 ms and then releasing it.

By default, RESET_N is pulled up internally. As the power domain of RESET_N is VCC_IO and the pin is pulled up inside the module, no external pull-up circuit is allowed for this pin.

An OC driver circuit as shown below is recommended to control the RESET_N pin.

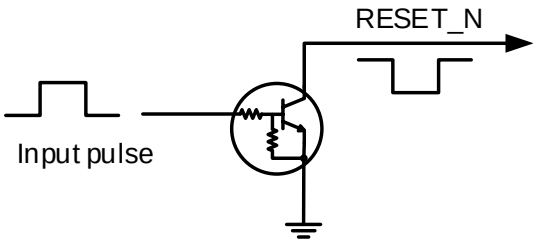


Figure 16: Reference OC Circuit for Module Reset

The following figure shows the reset sequence of the module.

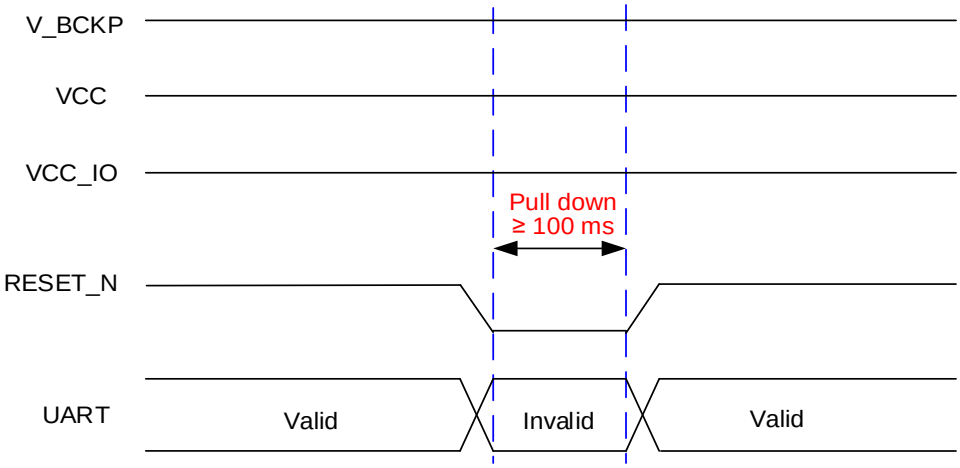


Figure 17: Reset Sequence

NOTE

1. RESET_N must be connected so that it can be used to reset the module if it enters an abnormal state.
2. Reset will force the loss of volatile RAM data, but the data in the non-volatile backup RAM won't be lost, so it is still possible to achieve fast TTFF.

5 Design

This chapter explains the reference design of RF section and recommended footprint of the module. GNSS receiver could be vulnerable to environmental interference. To learn the details about interference and ensuring interference immunity, see *document [6] GNSS antenna application note*.

5.1. Antenna Selection

5.1.1. Antenna Specifications

The modules can be connected to a dedicated passive or active single-band GNSS antenna to receive or track GNSS satellite signals. The recommended antenna specifications are given in the table below.

Table 8: Recommended Antenna Specifications

Antenna Type	Specifications
Passive Antenna	Frequency Range: 1559–1606 MHz Polarization: RHCP VSWR: < 2 (Typ.) Passive Antenna Gain: > 0 dBi
Active Antenna	Frequency Range: 1559–1606 MHz Polarization: RHCP VSWR: < 2 (Typ.) Passive Antenna Gain: > 0 dBi Active Antenna Noise Figure: < 1.5 dB Active Antenna Total Gain: < 35 dB [7]

NOTE

For recommended antenna selection and design, see *document [6] GNSS antenna application note* or contact Quectel Technical Support (support@quectel.com).

[7] The total antenna gain equals the internal LNA gain minus the total insertion loss of cables and components inside the antenna.

5.1.2. Antenna Selection Guide

Both active and passive single-band GNSS antenna can be used for the module. A passive antenna is recommended if the antenna can be placed close to the module. It is recommended to switch from a passive antenna to an active antenna once the loss is > 1 dB, since the insertion loss of RF cable can decrease the C/N_0 of GNSS signal. For more information about antenna selection, see *document [6] GNSS antenna application note*.

5.1.3. Active Antenna Reference Design

It is important to consider the operating voltage range of the antenna and the voltage drop on the power supply circuit. The voltage drop is caused by the resistor (R2) and the inductor (L1), MOSFET (Q1 which is only used in active antenna reference design with status detection) in the external power supply circuit.

To further mitigate the impact of out-of-band signals on GNSS module performance, you must choose the active antenna whose SAW filter is placed in front of the LNA in the internal framework. DO NOT place the LNA in the front.

5.1.3.1. Active Antenna Without Antenna Status Detection

The following figure is a typical reference design of an active antenna without antenna status detection. In this case, the antenna is powered by a separate 3.3 V power supply. When selecting the active antenna, it is necessary to consider the operating voltage range.

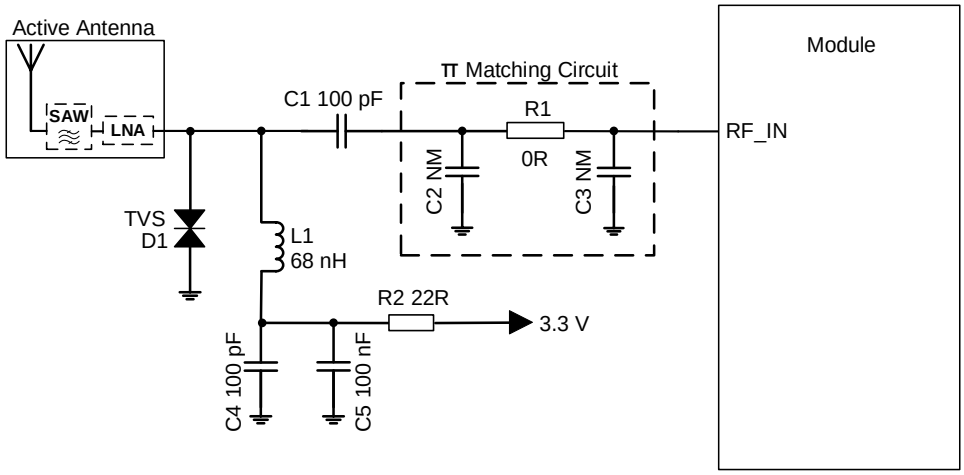


Figure 18: Active Antenna Reference Design Without Antenna Status Detection

C1 is a DC blocking capacitor used for blocking the DC current. C2, R1 and C3 components are reserved for matching antenna impedance. By default, R1 is 0 Ω, while C2 and C3 are not mounted; C1 is 100 pF; D1 is an electrostatic discharge (ESD) protection device to protect the RF signal input from the potential damage caused by ESD. The junction capacitance of D1 cannot exceed 0.6 pF and a transient voltage suppressor is recommended.

The inductor L1 is used to prevent the RF signal leakage into the separate power supply and to prevent noise propagation from the separate power supply to the antenna. The L1 inductor routes the bias voltage to the active antenna without losses. Place L1, C4 and C5 close to the antenna interface and route the proximal end of L1 pad on the RF trace. The recommended value of L1 should be at least 68 nH. The R2 resistor is used to protect the module in case the active antenna is short-circuited to the ground plane. RF trace impedance should be controlled to 50 Ω and traces should be as short as possible. For more information about RF layout, see *document [7] RF layout application note*.

5.1.3.2. Active Antenna with Antenna Status Detection

The following figure is a typical reference design of an active antenna with antenna status detection. In this design, short circuit or open circuit of antenna can be detected. When a short circuit is detected, the power supply of the antenna will be turned off immediately.

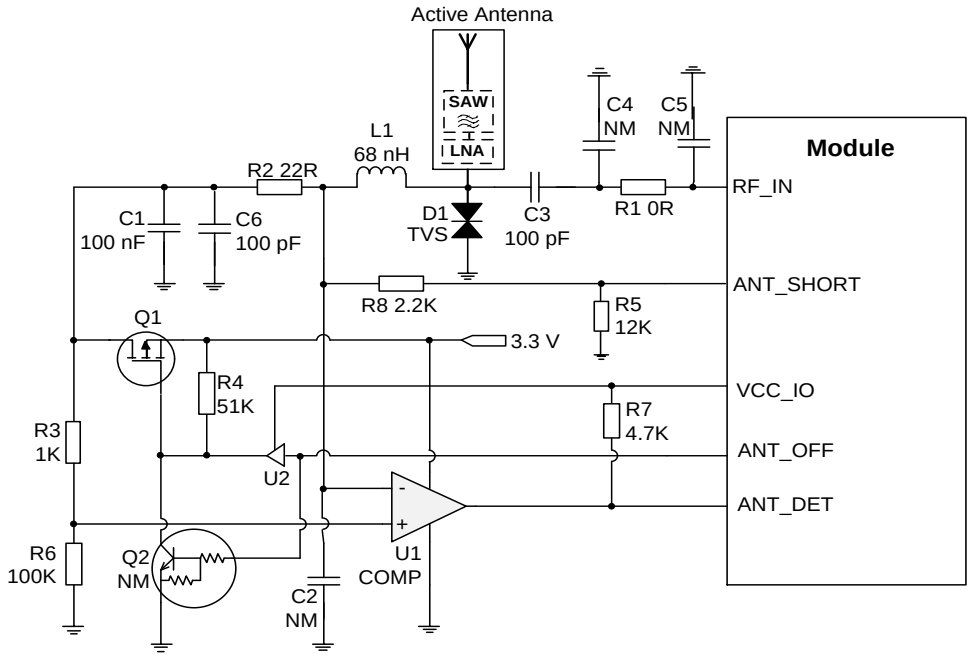


Figure 19: Active Antenna Reference Design with Antenna Status Detection

In the above reference design, the values of resistors R5 and R8 are applicable only when VCC = 3.3 V and VCC_IO = 2.8 V. For different VCC or VCC_IO voltage values, the values of R5 and R8 should be adjusted accordingly to ensure that V_{IH}nom (ANT_SHORT) = VCC_IO.

- The ANT_OFF pin is at a low level when the antenna is connected normally or is open-circuited, and is at a high level when the antenna is short-circuited. In this case, the circuit needs to mount U2, and the Q2 should not be mounted.
- The Q2 is designed to ensure compatibility and, therefore, is not generally mounted. To allow for possible software version upgrades, it is recommended to reserve Q2 in the circuit design.

NOTE

1. In the above design, the R2 resistor is mandatory; otherwise, the module may become permanently damaged because of the possible short-circuit of the active antenna.
2. The U1 is a universal open-drain output comparator. Quectel recommends ADCMP370 comparator from Analog Devices.
3. The U2 is a buffer, powered by the VCC_IO. The SN74LVC1G07DBV from Texas Instruments is recommended.

The active antenna status detection circuit includes two detection pins and one control pin. The control logic is shown in the table below.

Table 9: Active Antenna Detection Circuit Control Logic

Detection Pins		Control Pin	Antenna Status
ANT_SHORT	ANT_DET	ANT_OFF	
1	1	0	Normal
1	0	0	Open circuit
0	1	1	Short circuit

5.1.4. Passive Antenna Reference Design

The following figure is a typical reference design of a passive antenna.

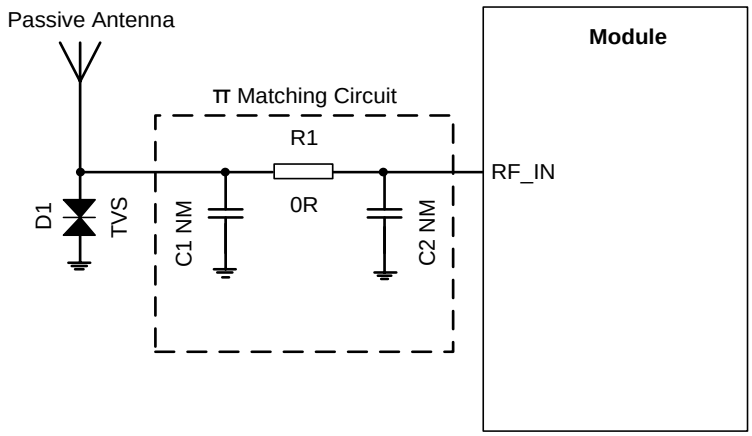


Figure 20: Passive Antenna Reference Design

C1, R1 and C2 components are reserved for matching antenna impedance. By default, R1 is 0 Ω, while C1 and C2 are not mounted. D1 is an electrostatic discharge (ESD) protection device to protect RF route from the damage caused by ESD. The junction capacitance of D1 cannot exceed 0.6 pF and a transient voltage suppressor is recommended. RF trace impedance should be controlled to 50 Ω and trace length should be as short as possible.

5.2. Recommended Footprint

The figure below describes module footprint. These are recommendations, not specifications.

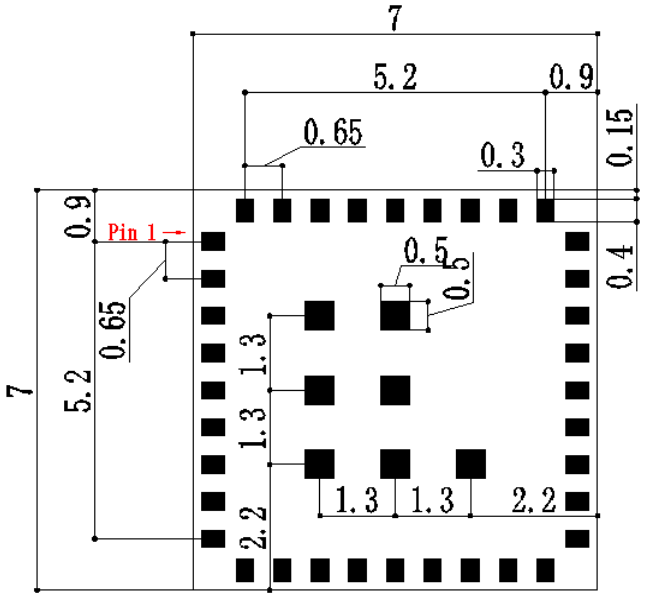


Figure 21: Recommended Footprint

NOTE

Keep at least 3 mm keepout between the module and other components on the motherboard to improve soldering quality and maintenance convenience.

6 Electrical Specification

6.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital pins of the module are listed in table below.

Table 10: Absolute Maximum Ratings

Parameter	Description	Min.	Max.	Unit
VCC	Main Power Supply Voltage	-0.3	4.3	V
V_BCKP	Backup Power Supply Voltage	-0.3	4.5	V
V_{IN}_IO	Input Voltage at I/O Pins	-0.2	3.1	V
P_{RF_IN}	Input Power at RF_IN	-	0	dBm
T_storage	Storage Temperature	-40	90	°C

NOTE

Stressing the device beyond the “Absolute Maximum Ratings” may cause permanent damage. The product is not protected against over-voltage or reversed voltage. Therefore, it is necessary to use appropriate protection diodes to prevent voltage spikes from exceeding the parameters specified in the table above.

6.2. Recommended Operating Conditions

The recommended operating conditions for the module are specified in the table below. It is important to note that, all specifications are based on an ambient temperature of +25 °C. Operating the module under extreme temperatures can significantly impact the specified values. Therefore, applications operating near the temperature limits should be tested to ensure the validity of the specification.

Table 11: Recommended Operating Conditions

Parameter	Description		Min.	Typ.	Max.	Unit
VCC	Main Power Supply Voltage		2.8	3.3	4.3	V
V_BCKP	Backup Power Supply Voltage		2.0	3.3	4.3	V
VCC_IO	Domain Voltage at Digital I/O Pins	1.8 V Domain	1.62	1.8	1.98	V
		2.8 V Domain	2.52	2.8	3.08	V
V_{IL}	Digital I/O Pin Low-level Input Voltage		-0.3	-	0.25 × VCC_IO	V
V_{IH}	Digital I/O Pin High-level Input Voltage		0.75 × VCC_IO	VCC_IO	VCC_IO + 0.3	V
V_{OL}	Digital I/O Pin Low-level Output Voltage		-0.3	-	0.15 × VCC_IO	V
V_{OH}	Digital I/O Pin High-level Output Voltage		0.85 × VCC_IO	VCC_IO	3.6	V
WAKEUP	Low-level Voltage		-0.3	-	0.275	V
	High-level Input Voltage		0.825	-	1.4	V
T_operating	Operating Temperature		-40	25	+85	°C

NOTE

1. Operating the device beyond the specified “Operating Conditions” is not recommended, and extended exposure beyond the “Operating Conditions” may affect device reliability.
2. Digital I/O Pin mentioned in the table above refers to all digital pins specified in *Table 6: Pin Description* except WAKEUP.

6.3. Supply Current Requirement

The following table lists the supply current values of the total system under various conditions. Actual power requirements may vary depending on processor load, external circuits, firmware version, the number of tracked satellites, signal strength, startup type, test duration and conditions.

Table 12: Supply Current

Parameter	Description	Condition	$I_{Typ.}$ [8]	I_{PEAK} [8]
I_{VCC} [9]	Current at VCC	Acquisition	24 mA	59 mA
		Tracking	23 mA	59 mA
		Standby mode	0.4 mA	0.45 mA
I_{V_BCKP} [10]	Current at V_BCKP	Continuous mode	0.16 mA	0.27 mA
		Standby mode	18 μA	52 μA
		Backup mode	6 μA	42 μA
I_{VCC_IO}	Current at VCC_IO	Continuous mode	0.46 mA	1 mA
		Standby mode	0.46 mA	0.5 mA
		Backup mode	0.3 mA	0.35 mA

6.4. ESD Protection

Static electricity occurs naturally and it may damage the module. Therefore, applying proper ESD countermeasures and handling methods is imperative. Consider the following measure to ensure protection against ESD damage when handling the modules:

- When mounting the module onto a motherboard, make sure to connect the GND first, and then the RF_IN pin.
- Avoid direct contact with any charged capacitors or materials that may easily generate or store charges (such as patch antenna, coaxial cable and soldering iron) when handling the RF_IN pin.
- When soldering the RF_IN pin, make sure to use an ESD safe soldering iron (tip) to prevent ESD-related damage.

[8] Room temperature, measurements are taken with typical voltage.
[9] Used to determine maximum current capability of power supply.
[10] Used to determine required battery current capability.

7 Mechanical Dimensions

This chapter provides the millimeter (mm) measurements of the module, including their mechanical dimensions. The dimensional tolerances are ±0.2 mm, unless otherwise specified.

7.1. Top, Side and Bottom View Dimensions

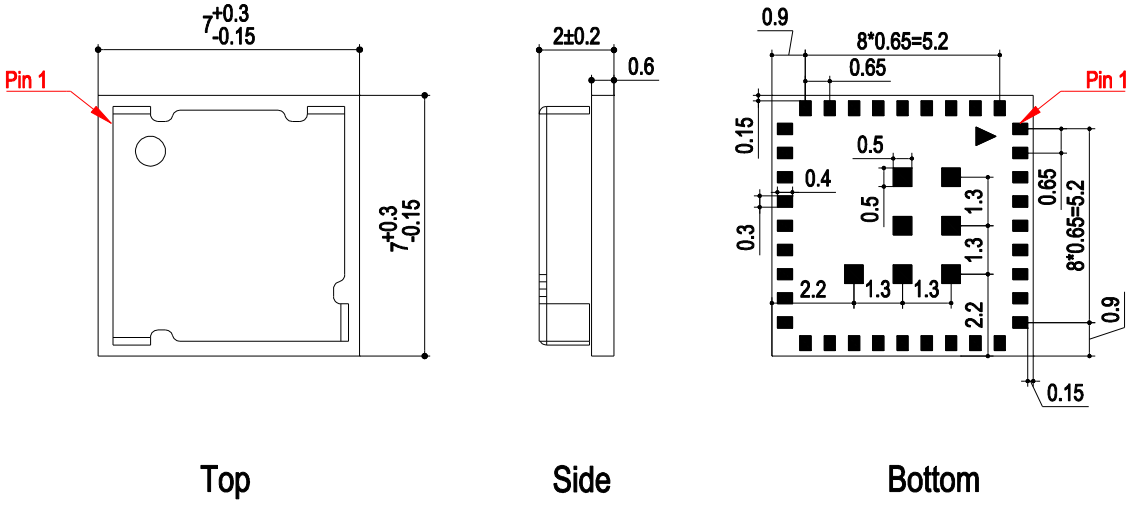


Figure 22: Top, Side and Bottom View Dimensions

NOTE

The package warpage level of the module conforms to the *JEITA ED-7306* standard.

7.2. Top and Bottom Views

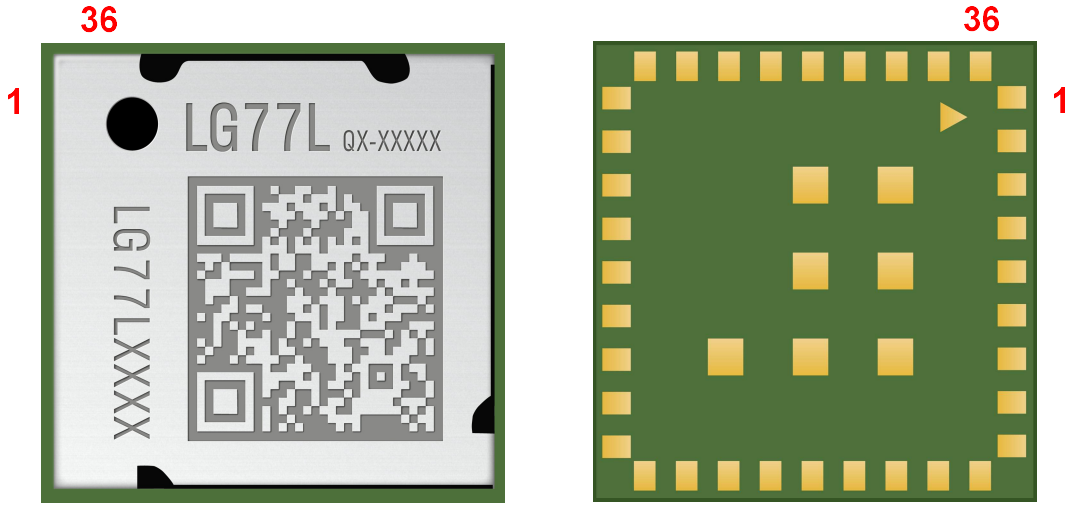


Figure 23: Top and Bottom View Dimensions

NOTE

The above images are for illustrative purposes only and may not reflect the actual representation of the module. For authentic representation, see the module received from Quectel.

8 Product Handling

8.1. Packaging Specification

This chapter outlines the key packaging parameters and process. All figures below are for reference purposes only, as the actual appearance and structure of the packaging materials may vary in delivery.

The modules are packed in a tape and reel packaging as specified in sub-chapters below.

8.1.1. Carrier Tape

Carrier tape dimensions are illustrated in the following figure and table:

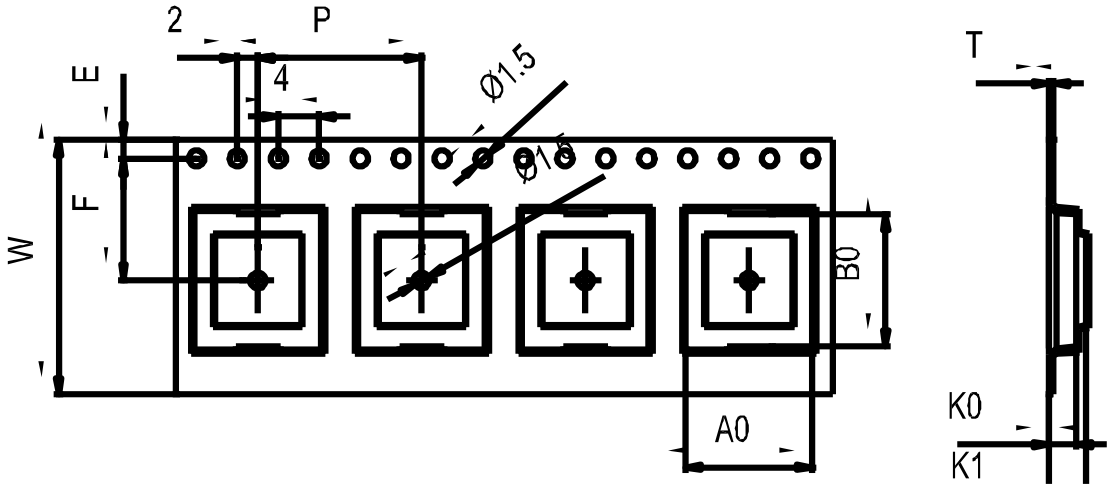


Figure 24: Carrier Tape Dimension Drawing (Unit: mm)

Table 13: Carrier Tape Dimension Table (Unit: mm)

W	P	T	A0	B0	K0	K1	F	E
24	16	0.4	7.4	7.4	2.5	3.5	11.5	1.75

8.1.2. Plastic Reel

Plastic reel dimensions are illustrated in the following figure and table:

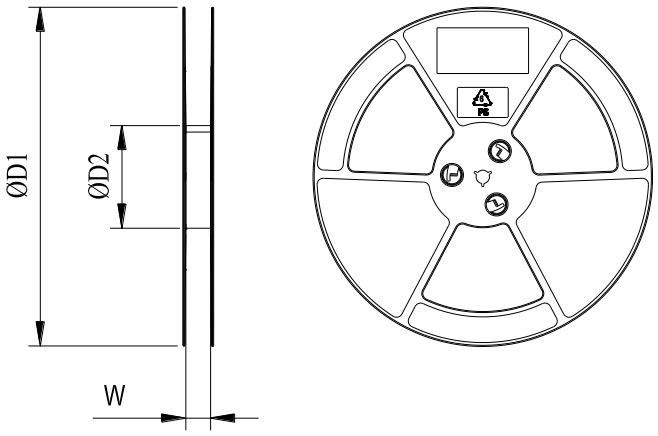


Figure 25: Plastic Reel Dimension Drawing

Table 14: Plastic Reel Dimension Table (Unit: mm)

øD1	øD2	W
330	100	24.5

8.1.3. Mounting Direction

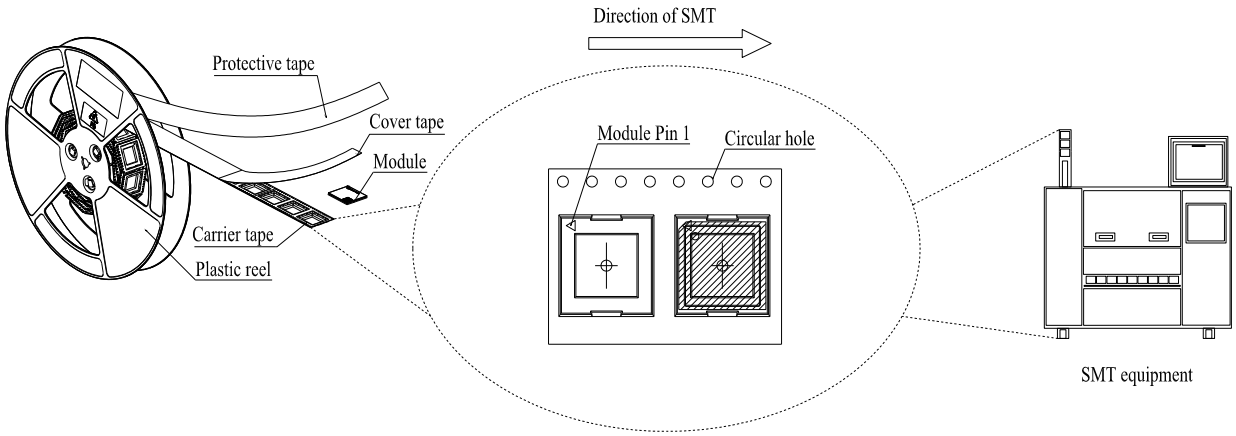
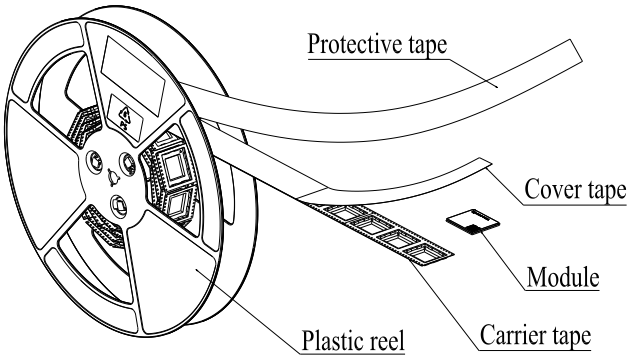


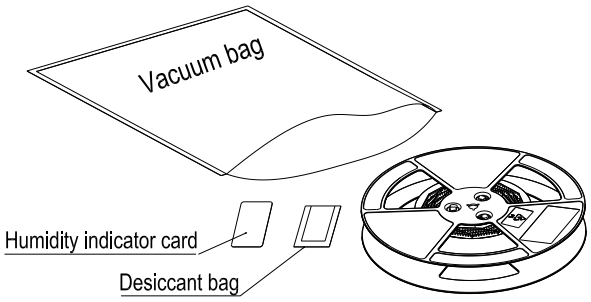
Figure 26: Mounting Direction

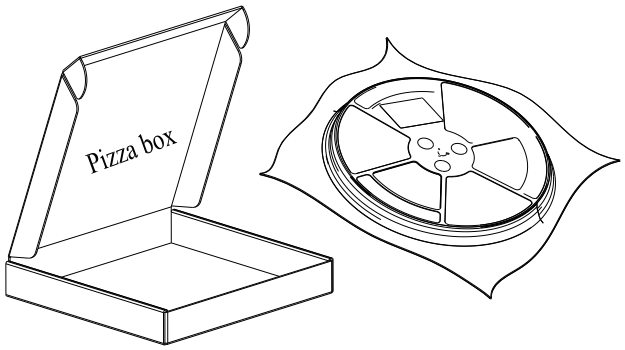
8.1.4. Packaging Process



Place the modules onto the carrier tape cavity and cover them securely with cover tape. Wind the heat-sealed carrier tape onto a plastic reel and apply a protective tape for additional protection. 1 plastic reel can pack 1000 modules.

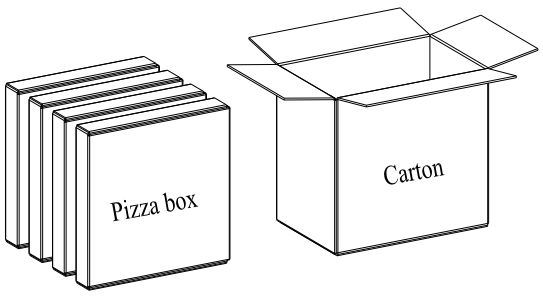
Place the packaged plastic reel, humidity indicator card and desiccant bag into a vacuum bag, and vacuumize it.





Place the vacuum-packed plastic reel into a pizza box.

Place the 4 packaged pizza boxes into 1 carton and seal it. 1 carton can pack 4000 modules.



Pizza box size (mm): 365 × 345 × 43
Carton size (mm): 380 × 190 × 365

Figure 27: Packaging Process

8.2. Storage

The module is provided in a vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: the temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.

2. Shelf life (in a vacuum-sealed packaging): 12 months in Recommended Storage Condition.

3. Floor life: 168 hours [11] in a factory where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g., a dry cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement mentioned above;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 8 hours at 120 ±5 °C;
   - The module must be soldered to PCB within 24 hours after the baking, otherwise it should be put in a dry environment such as a dry cabinet.

NOTE

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the module.

[11] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. Do not unpack the modules in large quantities until they are ready for soldering.

8.3. Manufacturing and Soldering

Push the squeegee to apply solder paste on the stencil surface, and ensure the paste fills the stencil openings and penetrates the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. For more information about the stencil thickness for the module, see *document [8] module SMT application note*.

The recommended peak reflow temperature should be 235–246 ºC, with 246 ºC as the absolute maximum reflow temperature. To avoid module damage from repeated heating, it is recommended to mount the module only after reflow soldering the other side of the PCB. The recommended reflow soldering thermal profile (for lead-free reflow soldering) and related parameters are shown in the figure and table below.

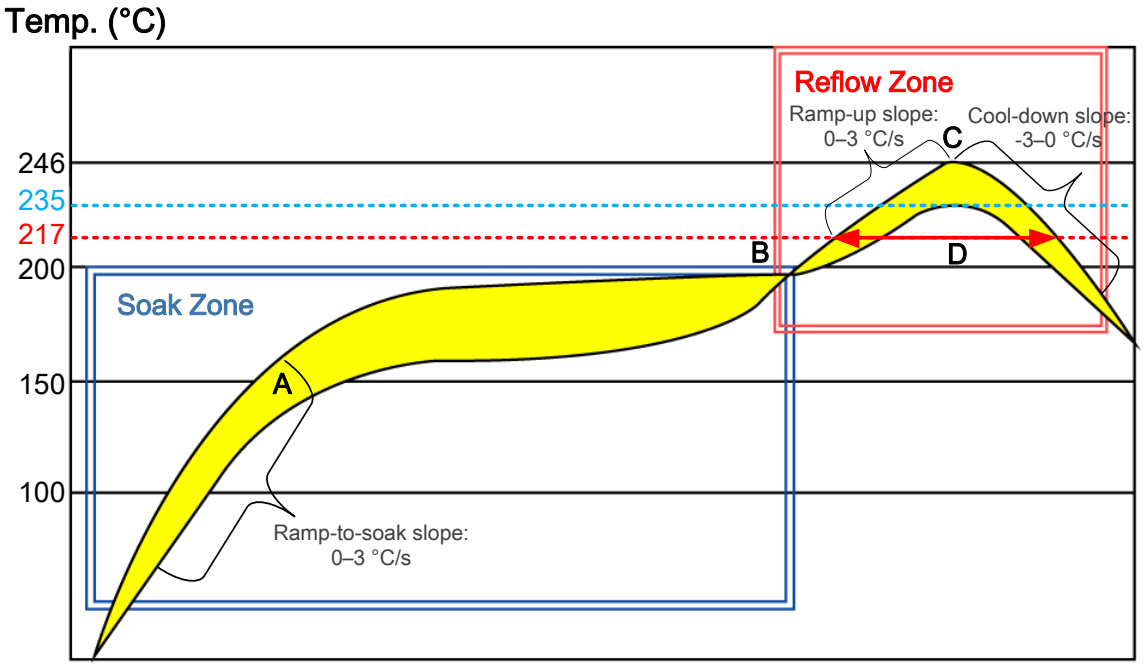


Figure 28: Recommended Reflow Soldering Thermal Profile

Table 15: Recommended Thermal Profile Parameters

Factor	Recommendation Value
Soak Zone	
Ramp-to-soak Slope	0–3 °C/s
Soak Time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
Ramp-up Slope	0–3 °C/s
Reflow Time (D: over 217 °C)	40–70 s
Max. Temperature	235–246 °C
Cool Down Slope	-3–0 °C/s
Reflow Cycle	
Max. Reflow Cycle	1

NOTE

1. The above profile parameter requirements are for the measured temperature of the solder joints. Both the hottest and coldest spots of solder joints on the PCB should meet the above requirements.
2. During manufacturing and soldering, or any other processes that may require direct contact with the module, **NEVER** wipe the module shielding can with organic solvents, such as acetone, ethyl alcohol, isopropyl alcohol, and trichloroethylene. Otherwise, the shielding can may become rusty.
3. The module shielding can is made of cupronickel base material. The Neutral Salt Spray Test has shown that after 12 hours the laser-engraved label information on the shielding can is still clearly identifiable and the QR code is still readable, although white rust may be found.
4. If a conformal coating is necessary for the module, **DO NOT** use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
5. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
6. Avoid using materials that contain mercury (Hg), as adhesives, for module processing, even if the materials are RoHS compliant and their mercury content is below 1000 ppm (0.1 %).
7. Corrosive gases may corrode the electronic components inside the module, affecting their reliability and performance, and potentially leading to a shortened service life that fails to meet the designed lifespan. Therefore, do not store or use unprotected modules in environments containing corrosive gases such as hydrogen sulfide, sulfur dioxide, chlorine, and ammonia.
8. Due to SMT process complexity, contact Quectel Technical Support in advance regarding any ambiguous situation, or any process (e.g., selective soldering, ultrasonic soldering) that is not addressed in *document [8] module SMT application note*.

9 Labelling Information

The label of the Quectel GNSS modules contains important product information. The location of the product type number is shown in figure below.

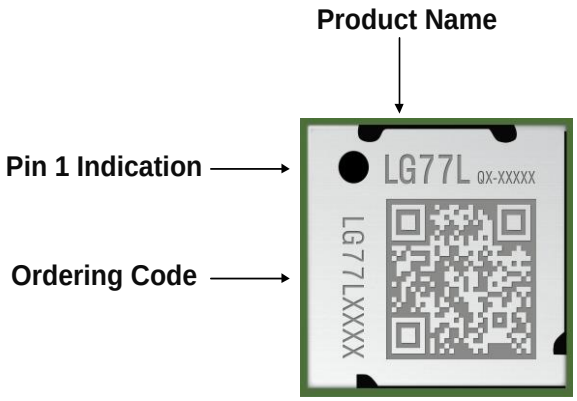


Figure 29: Labelling Information

The image above is for illustrative purposes only and may not reflect the actual appearance and label of the modules. For authentic representation, see the modules received from Quectel.

10 Appendix References

Table 16: Related Documents

Document Name
[1] Quectel_LG77L(C)&Lx0&Lx6&LC86L&Series_GNSS_Protocol_Specification
[2] Quectel_Lx0&Lx6&LC86L&LG77L_AGNSS_Application_Note
[3] Quectel_Lx6&LC86L&LG77L_Firmware_Upgrade_Guide
[4] Quectel_LG77L(C)_Reference_Design
[5] Quectel_Lx6&LG77L_I2C_Application_Note
[6] Quectel_GNSS_Antenna_Application_Note
[7] Quectel_RF_Layout_Application_Note
[8] Quectel_Module_SMT_Application_Note

Table 17: Terms and Abbreviations

Abbreviation	Description
1PPS	One Pulse Per Second
AGNSS	Assisted Global Positioning System
AIC	Active Interference Cancellation
ARM	Advanced RISC Machine
BDS	BeiDou Satellite Navigation System
bps	bits per second
C/N_0	Carrier-to-noise Ratio
DR	Dead Reckoning

Abbreviation	Description
EASY	Embedded Assist System
EGNOS	European Geostationary Navigation Overlay Service
EPO	Extended Prediction Orbit
ESD	Electrostatic Discharge
GAGAN	GPS Aided Geo Augmented Navigation
Galileo	Galileo Satellite Navigation System (EU)
GLONASS	Global Navigation Satellite System (Russian)
GLP	GNSS Low Power
GNSS	Global Navigation Satellite System
GPS	Global Positioning System
I/O	Input/Output
I2C	Inter-integrated Circuit
IC	Integrated Circuit
IMU	Inertial Measurement Unit
I_{PEAK}	Peak Current
NavIC	Indian Regional Navigation Satellite System
kbps	kilobits per second
LDO	Low-dropout Regulator
LGA	Land Grid Array
LNA	Low-noise Amplifier
MCU	Microcontroller Unit/Microprogrammed Control Unit
MSAS	Multi-functional Satellite Augmentation System (Japan)
MSL	Moisture Sensitivity Levels
NMEA	National Marine Electronics Association
OC	Open Connector

Abbreviation	Description
PCB	Printed Circuit Board
PI	Power Input
PMU	Power Management Unit
ppm	parts per million
PQ	Quectel Proprietary Protocol
PSRR	Power Supply Rejection Ratio
QZSS	Quasi-zenith Satellite System
RAM	Random Access Memory
RF	Radio Frequency
RHCP	Right Hand Circular Polarization
RoHS	Restriction of Hazardous Substances
ROM	Read Only Memory
RTC	Real-time Clock
RTK	Real-time Kinematic
RXD	Receive Data (Pin)
SAW	Surface Acoustic Wave
SBAS	Satellite-based Augmentation System
SCL	Serial Clock
SMD	Surface Mount Device
SMT	Surface Mount Technology
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
TCXO	Temperature Compensated Crystal Oscillator
T_operating	Operating Temperature
TTFF	Time to First Fix

Abbreviation	Description
TVS	Transient Voltage Suppressor
TXD	Transmit Data (Pin)
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
V_{Imax}	Maximum Input Voltage
V_{Imin}	Minimum Input Voltage
V_{Inom}	Normal Input Voltage
V_{IHmax}	High-level Maximum Input Voltage
V_{IHmin}	High-level Minimum Input Voltage
V_{ILmax}	Low-level Maximum Input Voltage
V_{ILmin}	Low-level Minimum Input Voltage
V_{OLmax}	Low-level Maximum Output Voltage
V_{OLmin}	Low-level Minimum Output Voltage
V_{OHmax}	High-level Maximum Output Voltage
V_{OHmin}	High-level Minimum Output Voltage
VSWR	Voltage Standing Wave Ratio
WAAS	Wide Area Augmentation System
XTAL	External Crystal Oscillator